RCA

Broadcast Equipment

TR-22, TR-3, TR-4
Television Tape Machines

Color Automatic Timing Corrector

ES-43581

ES-43582

IB-31652

Broadcast Equipment

Instructions

TR-22, TR-3, TR-4
Television Tape Machines

Color Automatic Timing Corrector

ES-43581

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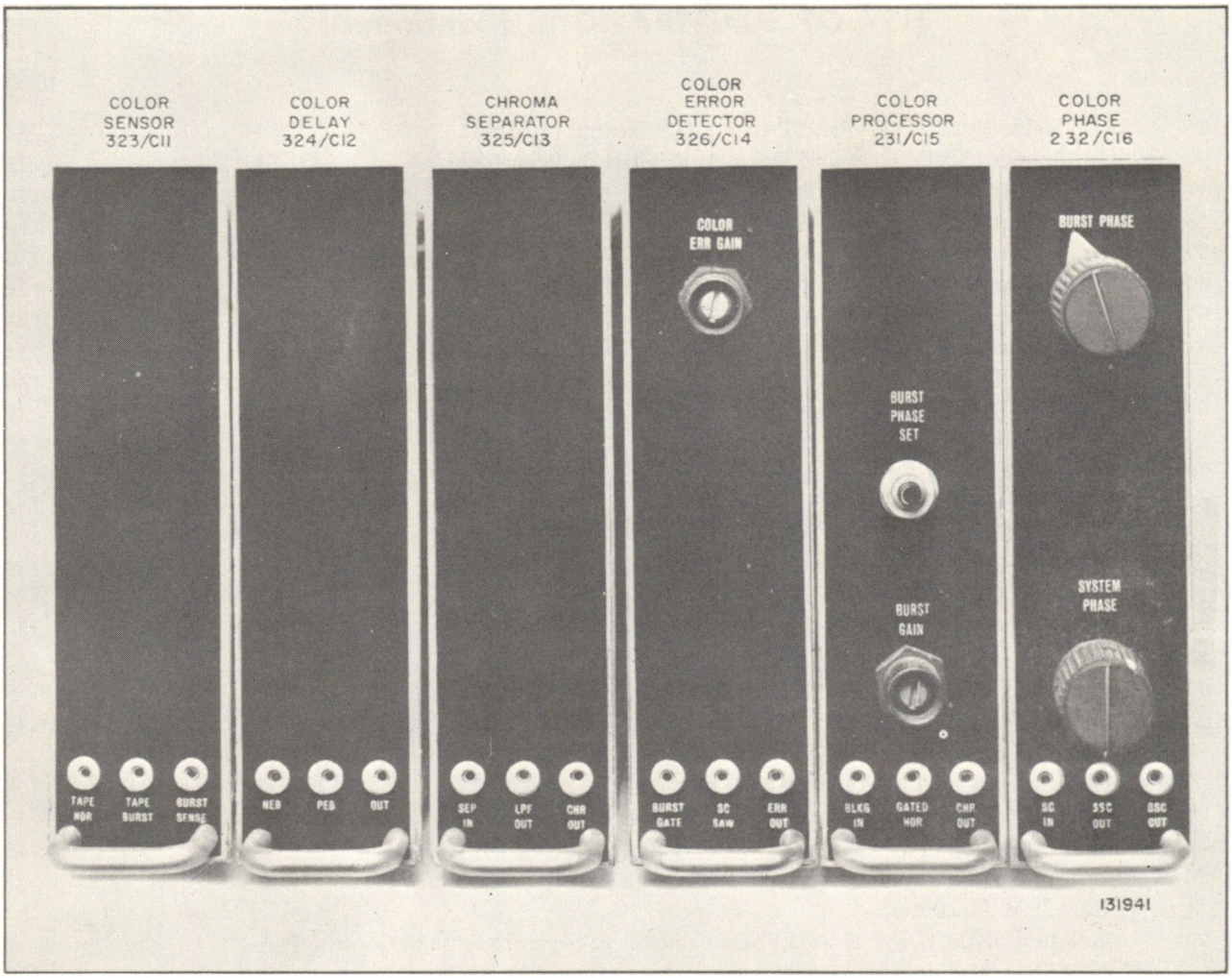


Figure 1—Color ATC Modules (MI-43353)

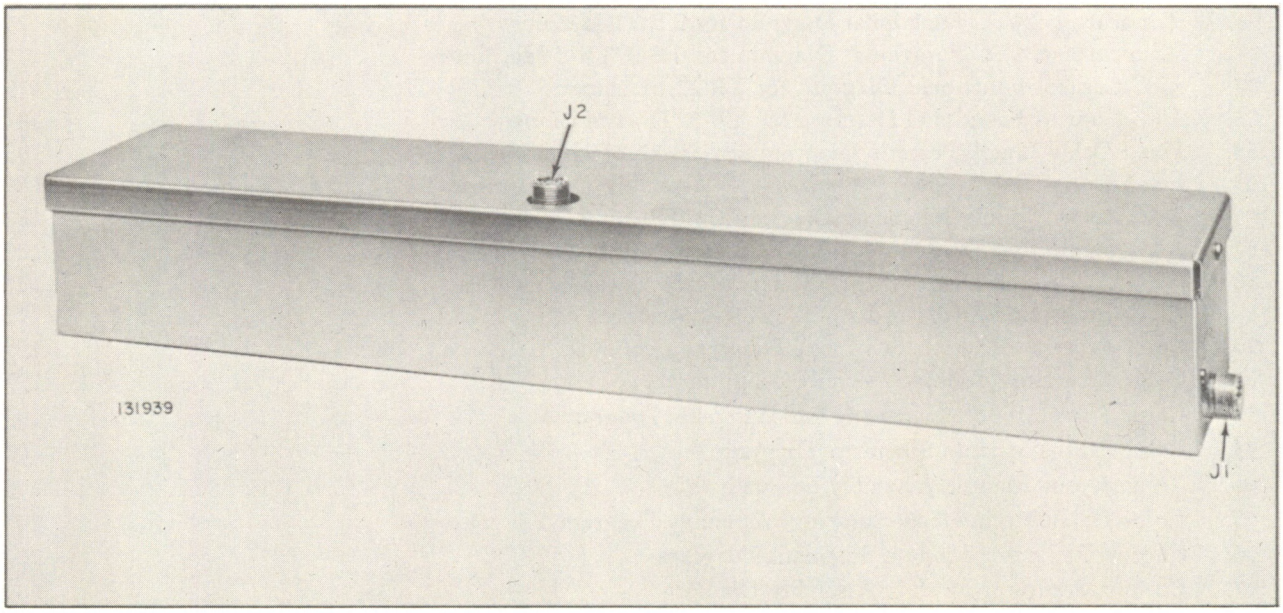


Figure 2—Color Fixed Delay Line for TR-22 Machines

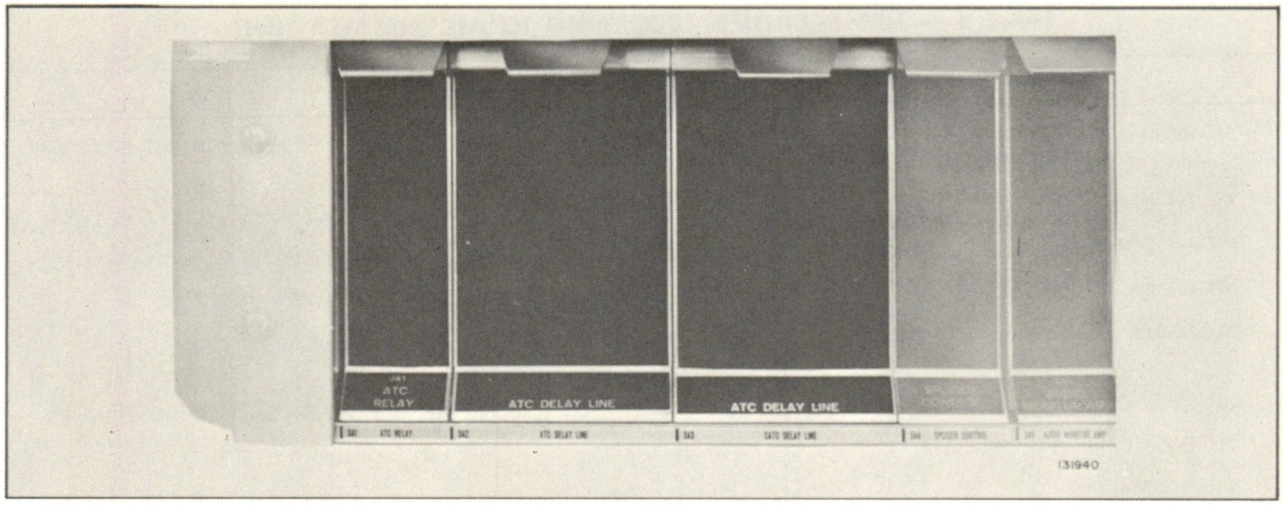


Figure 3—Color Fixed Delay Line Module for TR-3/TR-4 Machines

COLOR ATC SYSTEM

GENERAL DESCRIPTION

The function of the color ATC (automatic timing correction) system is to operate in conjunction with the monochrome ATC system in reducing timing errors to values which allow reproduction of an excellent quality color picture. The timing errors, if not reduced, produce effects in the picture which fall into the two general categories commonly referred to as geometric distortion and jitter. Geometric distortion includes various segmentation errors which result in picture distortions such as jogs, scallops, and indentations caused by video head quadrature error. Segmentation errors are sufficiently minimized for monochrome picture reproduction by the monochrome ATC system; however, optimum color reproduction requires a considerably greater error reduction. A comparison of segmentation error effects between monochrome and color reproduction may be made by observing the fact that a picture displacement from line-to-line of 0.03 microsecond is not visible in a monochrome picture but represents a 40-degree color subcarrier phase shift which in turn produces a serious hue shift in the color picture. Time-base jitter, inherent in all quadruplex recording processes, is caused by nonuniformities in the mechanical motions of the machine. The pixlock servo system is capable of reducing the residual jitter to a value of approximately 0.1 microsecond, which is satisfactory for monochrome operation but which represents a 130-degree subcarrier phase shift and is therefore intolerable for color.

Equipment Supplied

The color ATC system is available in kit form as an accessory which may be added to all RCA Television Tape machines of the TR-22, TR-3, or TR-4 series which have had the monochrome ATC system installed. The color ATC system consists of a fixed delay line and the following six modules:

Color Sensor (no. 323/C11), MI-40596
Color Delay (no. 324/C12), MI-40597
Chroma Separator (no. 325/C13), MI-40598
Color Error Detector (no. 326/C14), MI-40599
Color Processor (no. 231/C15), MI-40594
Color Phase (no. 232/C16), MI-40595

TR-22 machines require the ES-43581 color ATC system which contains MI-43353 and MI-40688. MI-43353 consists of the six color ATC modules (figure 1), and MI-40688 includes the color fixed delay line for TR-22 machines (figure 2). TR-3/TR-4 machines require the ES-43582 color ATC system which contains MI-43353 and MI-43392. MI-43353 consists of the six color ATC modules, and MI-43392 consists of the color fixed delay line module for TR-3/TR-4 machines (figure 3). Since the MI-43353 color ATC modules are utilized in TR-22 and TR-3/TR-4 series machines, the modules are interchangeable between machines of different series as well as between machines of the same series.

NOTE: The color ATC system requires machine operation in the pixlock servo mode. Therefore, TR-3 machines to serial no. 3151 and TR-4 machines to serial no. 4151 must be equipped with the optional pixlock servo facility, as well as with the monochrome ATC facility, for color ATC operation.

TABLE I — NPC FACILITIES ACCORDING TO ATC INSTALLATIONS

Equipment	*Serial No.*	*NPC Facilities*
MI-40690 ATC Harness and Monochrome ATC Modules	101 to 125 and 1001 to 1200	Require modification with MI-43311 kit
MI-43390 ATC Harness	All serial numbers	Require modification with MI-43311 kit
MI-43391 Monochrome ATC Modules	1301 - 1375	Require modification with MI-43311 kit
MI-43390A ATC Harness	All serial numbers	Factory wired for NPC
MI-43391A Monochrome ATC Modules	1201 through 1300 and 1376 up	Factory wired for NPC
MI-40693 Color ATC Modules	701 through 795	Require modification with MI-43312 kit
MI-43353 Color ATC Modules	796 up	Factory wired for NPC
TR-22C Machines[1]	1301 through 1375	Require modification with MI-43311 kit
MI-43352 ATC Harness for TR-3/TR-4 Machines	All serial numbers	Factory wired for NPC

[1] ATC Harness Factory Wired.

All ES-43581 and ES-43582 color ATC systems (serial nos. above 795) include the facility for NPC (non-phased color) operation. MI-40693 color ATC systems (serial nos. below 796) may be modified to include the NPC facility by the addition of the Color ATC Improvement Kit (MI-43397) and the NPC Modification Kit for Color ATC (MI-43312). Color ATC operation in the NPC mode requires that the monochrome ATC system also include the NPC facility. Some monochrome ATC systems are factory wired for NPC operation; those that are not must be modified by adding the NPC Modification Kit for Monochrome ATC (MI-43311) before the color ATC system may be operated in the NPC mode. Table I lists the various Television Tape equipments and indicates whether or not NPC modifications are required.

Installation

Installation of the ES-43581 and ES-43582 color ATC systems must be preceded by installation of the monochrome ATC system. All wiring required by the color ATC system is included in the monochrome ATC harness; thus, in most instances, installation of the color ATC system is merely a matter of inserting the modules and, in TR-22 machines, installing the color fixed delay line. The few color ATC system installation procedures required, as well as procedures for installation of remote system controls, are presented in the *Installation* section at the rear of this instruction book.

Operating Modes

Two operating modes are possible with the color ATC system. These are the normal color ATC mode and the non-phased color (NPC) mode. The normal color ATC mode is utilized only when playing back interlaced color (IC) tapes, which are first generation color tapes or direct color dubbed tapes. Interlaced color tapes allow horizontal as well as vertical phasing so that mixing, fading, or the incorporation of special effects may be attained. The NPC mode is utilized primarily when playing back non-interlaced color (NIC) tapes. Non-interlaced color tapes are tapes dubbed using a heterodyne playback system; therefore a fixed phase relationship between the color and monochrome signals is no longer maintained. The NPC mode may also be utilized when playing back interlaced color tapes or mixtures of interlaced and non-interlaced color tapes. However, playback in the NPC mode, whether of an interlaced or a non-interlaced tape, results in an output in which the horizontal phase relationship between tape sync and reference sync cannot be controlled. Therefore it is not possible to utilize special effects or to fade between the tape machine and other signal sources when playing back tape in the NPC mode. (It should be noted that playback of non-interlaced color tape results in a non-interlaced output signal.)

Color tape playback in either the normal color ATC mode or the NPC mode requires machine operation in the pixlock (or linelock) servo mode.

Color tape playback *cannot* be obtained with the machine operating in either the tonewheel or the switchlock servo mode. Therefore, TR-3 and TR-4 machines for which the pixlock operation is optional must have this servo mode added before color tape may be played back. Color tape may be played back in the linelock servo mode only in machines equipped with the optional linelock only (LLO) facility.

The linelock servo mode allows horizontal "locking" but does not require vertical phasing. This mode of servo operation is especially advantageous during playback of tapes where vertical phasing is not critical, since recovery from interruptions will be faster than the recovery during full pixlock operation.

OPERATING PROCEDURE

An initial color ATC system setup adjustment procedure is provided in the *System Adjustments* section of this instruction book. Once the machine has been initially set up according to these procedures, color tapes may be played back by simply rotating the selector switch on the monochrome ATC delay/output module (no. 223/B11) to select the desired color ATC operating mode (normal color ATC or non-phased color) and, if required, making slight adjustments of the BURST PHASE and/or SYSTEM PHASE controls located on the color phase module (no. 232/C16) front panel.

The BURST PHASE control is utilized in adjusting the system to obtain a proper color picture, containing natural flesh tones, etc. The control is set by adjusting it during color tape playback so that color bars appearing on the color monitor with the VID OUT pushbutton on the picture monitor switcher depressed are identical in shading to the color bars appearing on the monitor when the VID IN pushbutton is depressed.

The SYSTEM PHASE control acts as a cable length compensating device and its purpose is to make it possible to precisely adjust the phase of the tape machine output so that when mixing various color signal sources the phase of each is identical with respect to that of a reference. The control is set by simply adjusting it when mixing various color signal sources (e.g., live and tape color signals) so that the phase of each source is identical with respect to that of a reference.

DISCUSSION OF BASIC ATC SYSTEMS

General

The function of an ATC system, as it is utilized in television tape machines, is to correct timing errors. Correction of timing errors allows almost perfect time base stability in the reproduced picture without the need for constant attention and critical manual adjustments. Time base instability is introduced by the mechanical scanning process in quadruplex television tape machines, and appears in the reproduced picture in two forms which are generally referred to as geometric distortion and jitter.

Geometric distortion is caused mainly by the process of segmenting the picture signal into 16- or 17-line groups for recording on the various tracks on tape. This type of distortion is due to rapid timing errors which cause regular horizontal displacements of various portions of the picture. The distortion takes the following three forms: (1) steps, or uniform horizontal displacement of groups of lines due to quadrature errors in the headwheel; (2) jogs, or a "skewed" pattern caused by misalignment of the vacuum guide in a direction parallel to the headwheel panel; (3) scallops, or bows, caused by misalignment of the vacuum guide in a direction perpendicular to the headwheel panel.

The ATC system completely corrects steps (such as the errors resulting from improper headwheel quadrature) because the timing error remains constant throughout the length of each individual line. The ATC system also corrects jogs (skewing), because the timing error from jogs, although increasing throughout each line, increases at a constant rate and is the same for corresponding points on successive lines. (A skewed picture passing through any ATC type system has a small, constant error at its right-hand side, however this error is not visible in the reproduced picture.)

Errors resulting from scalloping cannot be completely removed by an ATC type system because the timing error at the right-hand side of the picture is not the same for successive lines. The difference in timing errors for successive lines will be seen in the ATC output as a small "skew-like" effect in vertical lines at the right-hand side of the picture only. It is therefore essential that the mechanical scalloping adjustment on the headwheel panel be performed carefully.

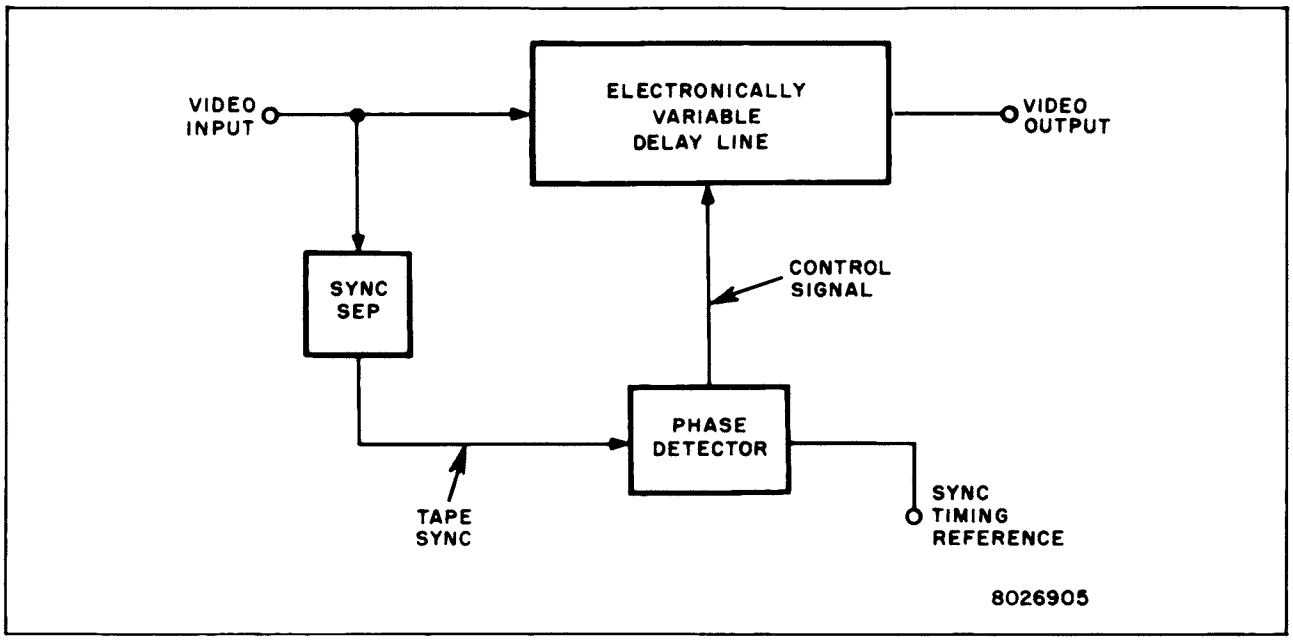


Figure 4—Open-Loop Principle of Monochrome ATC System

The electronically variable delay line, based upon the properties of silicon diode capacitors and controlled by time base error measuring circuits, provides a sufficient correction range to achieve non-critical machine operation. Measurement of time base error is accomplished by phase detector circuits which compare the timing of the video synchronizing information (sync) and a suitable timing reference. An open-loop control system, capable of one-line response, is utilized in the ATC system so that the variable delay line is able to change its delay by the full range from one line to the next.

Monochrome ATC

In the basic monochrome ATC system, the demodulated video signal is passed through an electronically variable delay line which is controlled by an error signal derived from the phase comparison of horizontal sync with a suitable timing reference (figure 4). A single-ended video signal is fed to the electronically variable delay line; however, control of the delay line is push-pull so that transients which are coupled from the control busses to the video path by the capacitance of the diodes each time the control voltage changes will be balanced out.

Since the delay line is utilized in an open-loop control system, it is essential that the delay vs. input voltage characteristic be highly linear so that proper tracking of the control voltage over the entire delay range may be maintained. The capacitance vs. voltage characteristic of the silicon diode is highly non-linear, and a further non-linearity is introduced by the fact that delay varies as the square-root of capacitance. To correct for the non-linear effects, a non-linear amplifier is inserted into the delay line control path.

The diodes of the variable delay line represent a capacitive load and, for proper operation of the delay line, a fairly rapid response must be achieved, during which time the positive and negative error busses must remain accurately balanced so that transients coupled to the video signal will cancel. In addition, since the error driver amplifiers provide the ground return for the capacitors of the delay line, the drivers must present a negligibly low impedance to the line over the entire video pass band. These conditions are met by the combination of complementary symmetry emitter followers on each error bus and an additional fixed capacitance which provides the higher video frequencies with a low impedance path to ground.

As the diode capacitance is modulated, both the delay and the characteristic impedance of the delay line will change. The line is terminated at both ends with fixed resistances which are accurately matched to the line impedance at the center of the delay range. Thus as modulation away from the center of the delay range takes place, an increasing mis-termination results. The total amount of delay modulation which can be achieved by a line of given length must therefore be limited so that the reflections produced by mis-termination are never great enough to become visible in the picture.

Since a large timing shift may occur when the machine switches from one video head to another during the playback process, it is essential that head switching take place *before* the timing error is measured to set the delay for the next line. Head switching in RCA television tape machines occurs during the horizontal interval; thus the trailing edge of horizontal sync is utilized for delay error measurement by the monochrome ATC system. (See figure 5.) The delay-change transient must be contained within the width of horizontal sync so that it does not interfere with either the timing of the leading edge of sync (which is utilized by TV receivers) or color burst which appears immediately after the trailing edge of sync. It is inherent that the delay-change transient in such a variable delay line cannot be shorter than the delay of the line itself, and in actuality the transient is longer than this because of rise time limitations in changing the amplitude of the control voltage fed to the delay line. Therefore, to produce a delay-change transient which is sufficiently short to fit within the horizontal sync interval, the delay line is split into two sections with each section having a separate control circuit. A fixed delay inserted into the video path before the video signal enters the split variable delay line causes the delay-change transient in the resultant signal from the delay line to occur ahead of the sync edge which is measured to produce the delay change.

The monochrome ATC system as described above is capable of reducing timing errors by a factor of at least 25:1. This is a sufficient error reduction for reproduction of an excellent quality monochrome picture. Color reproduction, however, requires a substantially greater error reduction.

Color ATC

The preceding paragraphs discuss the basic considerations of an ATC system which operates effectively with monochrome signals. For color operation however, additional considerations must be taken into account. One of these is noise. When horizontal sync is utilized in video signal timing measurement, only one sample per TV line is provided and a relatively wide bandwidth is required to pass the signal. Therefore, the timing measurement will be affected by the random noise which is added by the tape recording process, thus producing an effect known as *positional noise*. Positional noise is at or below the threshold of visibility during monochrome operation and is therefore not critical; however, during color operation positional noise represents a substantial phase jitter which results in phase instability. The color

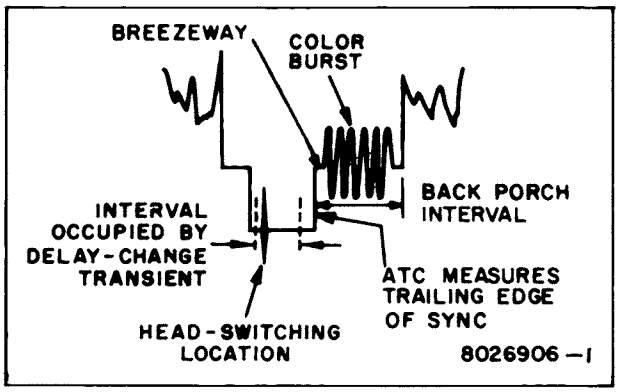


Figure 5—Locations of Head Switching and ATC Delay-Change Transients

ATC system reduces the effect of positional noise because of the availability of a greater number of samples per TV line (due to approximately eight cycles of subcarrier in the burst) and because of the possible use of a narrower bandwidth.

A second factor which prohibits the use of horizontal sync phase comparison in color operation is that there is no specified phase relationship between the edge of sync and the color subcarrier. In addition, it is possible that time modulation may be introduced between horizontal sync and the color subcarrier. Thus horizontal sync cannot be utilized in controlling the absolute phase of the subcarrier, and it is therefore essential that the final color timing correction be accomplished by comparing the phase of burst with a fixed reference.

As mentioned previously, the open-loop system is capable of maintaining an error reduction factor of at least 25:1, which is sufficient for monochrome reproduction but which may leave enough residual error to disrupt color performance if large errors are being corrected by monochrome ATC. Because of the cascading effect of the color ATC process, the residual error may theoretically be reduced by another factor of 25:1, and any error remaining is then negligible even for color operation.

The color ATC system employs the same open-loop control which has been described above for monochrome signals; however in the color system the error detector utilizes burst instead of horizontal sync. Also, the color ATC system requires a delay range of only 360 degrees at the subcarrier frequency (0.28 microsecond at a subcarrier frequency of 3.58 mc), therefore the delay line is shorter than that utilized in the monochrome ATC system and thus need not be split to contain the delay-change transient within the horizontal sync interval. The color

ATC non-linear amplifier, fixed delay line, and driver circuits are identical to those in the monochrome ATC system.

In the color ATC system it is necessary that the phase error detector have the equivalent of a linear delay range of 360 degrees at the subcarrier frequency. Design limitations prevent the detector from functioning effectively over an entire 360 degree delay range, thus the detector is operated at half-frequency and the required 360 degree delay range then appears to the detector as a 180 degree range. Multivibrators divide both the burst and the reference subcarrier signal, and the divided burst is utilized in forming narrow sampling pulses while the reference signal forms a sawtooth waveform. A special inhibit circuit in the burst path insures that the narrow sampling pulses will always sample on the center half of the sawtooth waveform slope.

The control signal for the color ATC variable delay line is formed in the color phase detector circuit by the measurement of burst phase error, and its function is to correct the phase errors in the composite color signal and thereby stabilize the signal timing to provide excellent color reproduction. However, the color signal must still be passed through the processing amplifier circuitry of the machine to clean up blanking and sync and insert a new color burst that is free of noise. This requires special circuitry which will not distort the color components of the signal.

The system utilized in processing the color signal consists of splitting the composite color signal into high-pass and low-pass components. The low-pass component does not contain any color information and thus may be passed through the standard monochrome processing amplifier circuits to clean up blanking and sync. The high-pass signal contains all chroma information and is processed by special circuits in the color ATC system to clean up the blanking interval and insert regenerated burst. The high-pass signal is then added back to the low-pass signal just ahead of the output amplifier in the processing amplifier circuitry.

Color ATC thereby provides time base corrections in the tape playback signal to a residual error level of a few nanoseconds with respect to the subcarrier reference signal. This allows color tape recording with essentially no bandwidth or color response limitations. Thus the machine equipped with color ATC can record and play back color program material which is indistinguishable from the original live signal.

SYSTEM FUNCTIONAL DESCRIPTION

The following discussion is intended to explain in general terms the various functions performed by the color ATC system as it operates in conjunction with the monochrome ATC system in TR-22 and TR-3/TR-4 Television Tape Machines. Since the color ATC system is effectively an extension, or refinement, of the monochrome ATC system, and thus can become operational only after the monochrome ATC system has been incorporated into these machines, it is assumed that the customer is generally aware of the basic principles of automatic timing correction systems. These principles, as well as an extensive discussion of the monochrome ATC system, may be found in the monochrome ATC instruction book (IB-31661).

Additional diagrams which will prove useful in understanding the operation of the color ATC system are located at the rear of this instruction book and include the following:

Functional Block Diagram, Monochrome ATC System for TR-22 Machines, figure 80.

Functional Block Diagram, Monochrome ATC System for TR-3 and TR-4 Machines, figure 81.

Functional Block Diagram, Color ATC System for TR-22 Machines, figure 78.

Functional Block Diagram, Color ATC System for TR-3 and TR-4 Machines, figure 79.

Functional Diagram, ATC Control System for TR-22 Machines, figure 82.

Functional Diagram, ATC Control System for TR-3 and TR-4 Machines, figure 83.

For a detailed description of any specific portion of the color ATC system refer to the individual module circuit description.

Video Circuits

During color tape playback the video signal from the demodulator output module is fed to a 2.5 microsecond fixed delay line in the monochrome ATC system and then to the monochrome variable delay line in the monochrome ATC delay/output module, as shown in figure 6. The electronically variable delay line in the monochrome ATC delay/output module consists of two sections. The delay of the first section is controlled by the monochrome PEB (positive error bus) and NEB (negative error bus) potentials and the delay of the second section is controlled by the DPEB (delayed positive error bus) and DNEB (delayed negative error bus) potentials. Each section

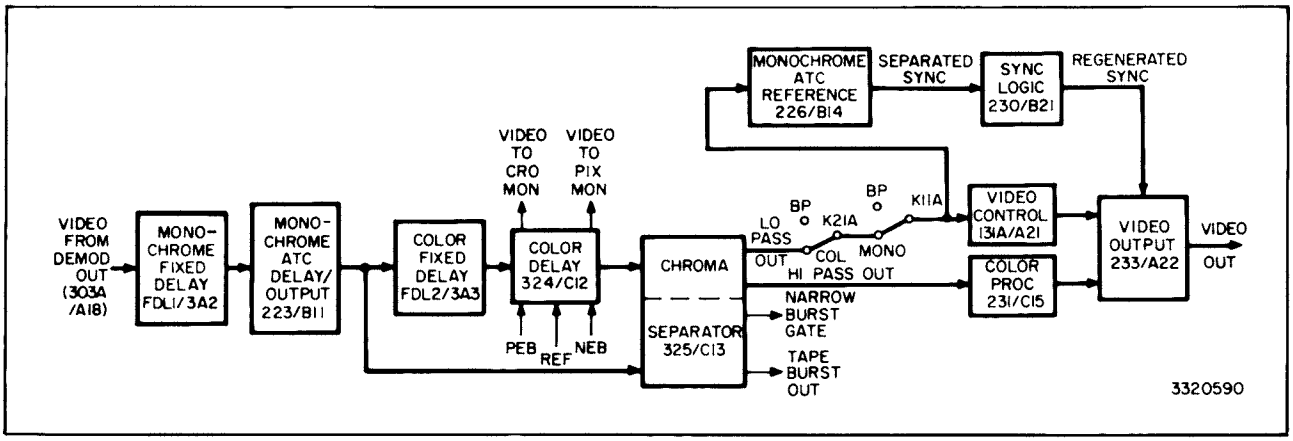


Figure 6—Video Path Through ATC Systems

provides a delay of 1.5 ±.25 microseconds; therefore the total delay inserted into the video path by the monochrome variable delay line varies from a minimum of 2.5 microseconds to a maximum of 3.7 microseconds and has a mid-range value of approximately 3.1 microseconds. The delayed video signal is fed from the monochrome ATC delay/output module to the color ATC system where it is applied to the chroma separator module and the color fixed delay line simultaneously.

The color fixed delay line inserts an additional 2.5 microsecond delay into the video signal path, and the output from the fixed delay line is fed to the electronically variable delay line in the color delay module. The variable delay line is controlled by the color PEB and NEB potentials which in turn are developed from a phase comparison of tape burst and reference subcarrier signals in the color error detector module. The phase comparison process results in transients which appear on the error busses. However, since the tape burst information, from which the sample pulses are derived, is obtained before the video signal has been delayed by the color fixed delay line (see figure 6), the transients applied to the variable delay line will be advanced 2.5 microseconds with respect to the video signal applied to the line. Therefore the transients will occur during the horizontal sync pulse interval and thus will not affect burst or video information in the composite signal. The output of the variable delay line is then the composite video signal which has been stabilized in time with respect to the reference subcarrier. This signal is fed to the chroma separator module and, in TR-22 and TR-4 machines, to the CRO and picture monitors.

Circuitry in the chroma separator module separates the low frequency and the high frequency (chroma) components of the delayed video signal so that they may be independently processed before being recombined. The separated high frequency (chroma) signal is fed to special processing circuitry in the color processor module. Special processing circuitry for the high frequency signal is required because the monochrome processing amplifier circuits will clamp out the burst signal and the black clipper will remove all signal components below black level. The low frequency signal is fed to the monochrome ATC reference module and to the monochrome processing circuits in the video control module, via the color and monochrome bypassing relays K21 and K11 which are energized during color tape playback in the normal color ATC or NPC (non-phased color) modes. Circuitry in the monochrome ATC reference module separates sync from the low pass signal, and the separated sync is utilized in the development of regenerated sync in the sync logic module. Regenerated sync is fed to the video output module where it is combined with the low pass and high pass portions of the video signal, which have been processed by circuitry in the video control and color processor modules respectively, to form the video output signal.

Burst Circuits

As shown in figure 7, the reference (local) 3.58 mc subcarrier signal is fed to the color phase module which contains two electronically variable delay lines. The delay of the first variable delay line is controlled by the SYSTEM PHASE control and may be varied over a range of nominally 0.3 microsecond (i.e., a delay equivalent to a subcarrier phase shift in excess of 360 degrees). Following this delay the reference subcarrier signal is fed simultaneously to the second variable delay line in the color phase module and to the color error detector module. The second variable delay line is controlled by the BURST PHASE control and the delay range available is also nominally 0.3 microsecond. The reference subcarrier delayed by

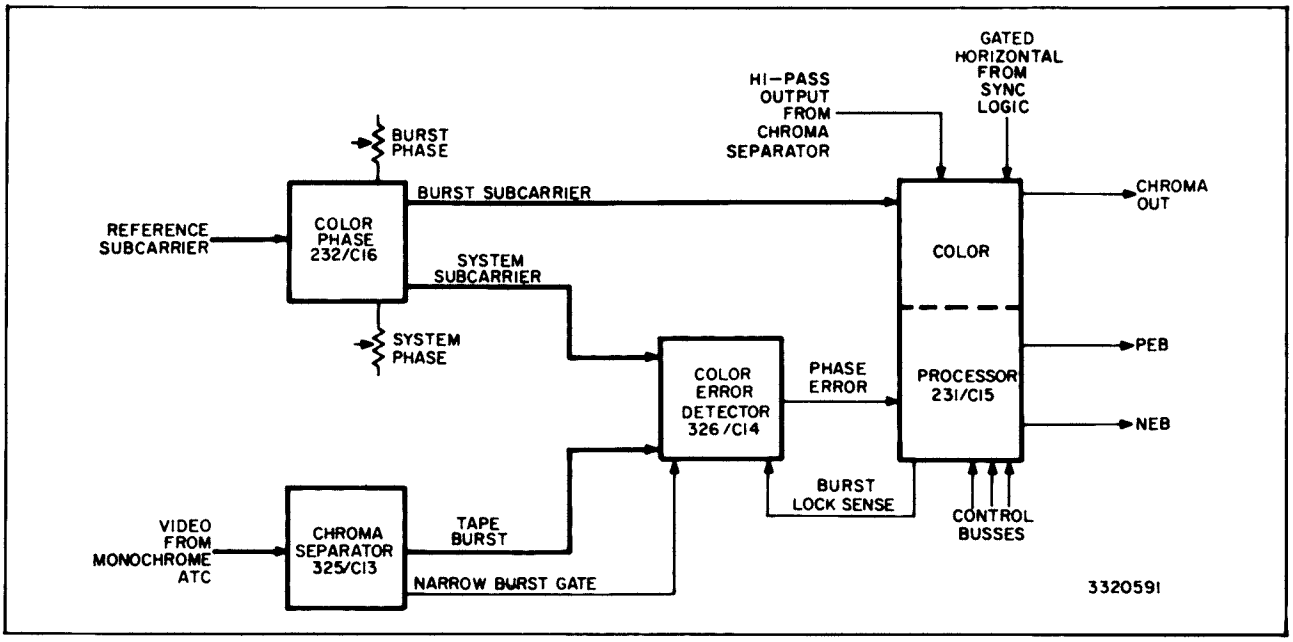


Figure 7—Burst Path Through Color ATC System

the second variable delay line is designated the burst subcarrier and is fed to the color processor module. The reference subcarrier fed directly to the color error detector module is designated the system subcarrier.

Tape burst, separated from the video signal in the chroma separator module, is also fed to the color error detector module. In the color error detector module the system subcarrier signal is utilized in generating a reference sawtooth waveform, while the tape burst signal is utilized in developing a sample pulse. The sample pulse and sawtooth waveform are fed to a phase comparator circuit where the sample pulse samples higher or lower on the sawtooth waveform slope, depending upon the relative phase between the reference subcarrier and tape burst signals. The output from the phase comparator circuit is thus an error signal whose magnitude reflects the difference in phase between the system (reference) subcarrier and tape burst signals. Logic circuits insure that sampling will occur only over the linear portion of the sawtooth waveform slope, and therefore the gain of the error detector is linear. If the sample pulse is sampling near either extreme of its range on the sawtooth waveform slope it is possible to obtain a "cracking effect" (i.e., successive pulses sampling at alternate extremes of the slope and thus producing conflicting error information). To prevent this effect during normal tape playback in the color ATC mode, a portion of the phase error signal is utilized in controlling the THAF (tape horizontal alignment, fine) signal in the color ATC system and the THAF signal in turn adjusts the video delay slightly so that the sample pulse will sample near the center of the sawtooth waveform slope.

The burst logic circuit which controls the sampling process is in turn controlled by the narrow burst gating pulse developed in the chroma separator module. The width of this pulse is variable; however, the width is nominally set at that value which allows approximately five samplings during each TV line. Thus the output error signal fed to the color processor module is a fluctuating series of d-c potentials. To eliminate the possibility of an erratic output signal, such as could occur if tape burst were suddenly lost, a clamping circuit provides a steady d-c output signal which corresponds to zero error if for any reason the tape burst signal is absent. The clamping circuit is controlled by the burst lock sense potential which in turn is determined by a logic circuit in the color processor module. The phase error signal fed to the color processor module is compared with a fixed reference in a differential amplifier circuit, and the resulting output is developed into the PEB and NEB potentials which control the variable delay line in the color delay module.

The color processor module contains circuitry which clamps the high-pass (chroma) signal from the chroma separator module during specific intervals according to the operating conditions of the machine, so that regenerated portions of the signal may be inserted later. When the machine is playing back a

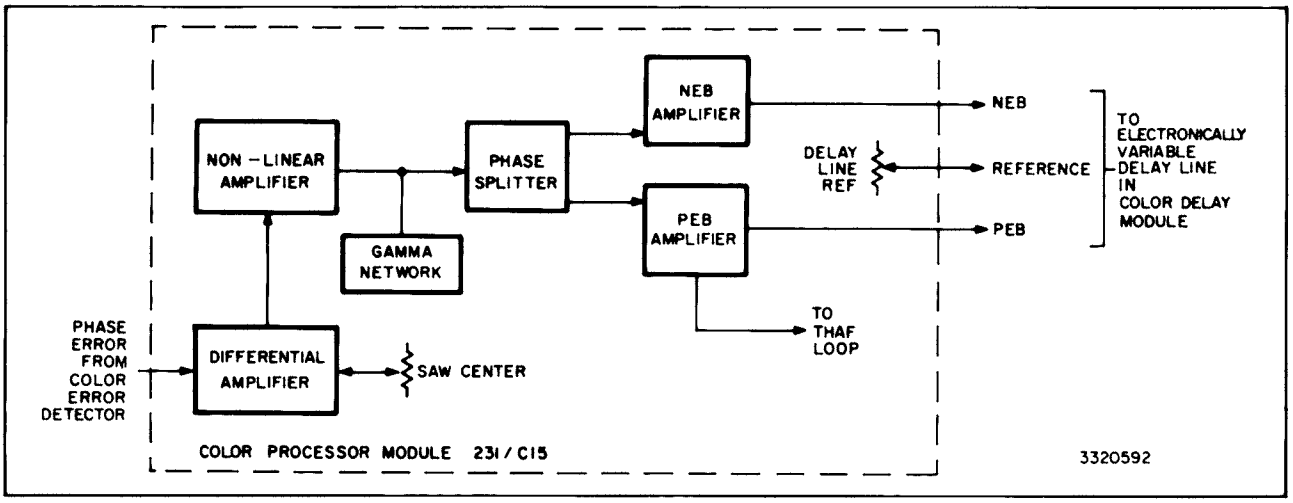


Figure 8—Development of PEB and NEB Potentials

color tape while "locked" in the pixlock (or linelock) servo mode the entire blanking interval is clamped, thus allowing the insertion of regenerated burst and regenerated sync. When the machine is operating in the STOP (MOD-DEMOD) mode, or is playing back a color tape in a non-pixlock (or linelock) servo mode, only the sync interval is clamped and the chroma output signal contains original burst. Regenerated burst, added to the high-pass signal during playback in the pixlock servo mode, is obtained by separating a portion of the burst subcarrier signal fed to the color processor module from the color phase module. Separation is accomplished by utilizing a diode bridge controlled by gating pulses timed to gated horizontal. The gating pulses insure that the proper number of cycles of burst are separated and that separation is timed so that regenerated burst will occur at precisely the correct moment to obtain a breezeway interval of 0.5 microsecond. If for any reason the machine fails to achieve a "lock" in the pixlock (or linelock) servo mode, a burst killer circuit disables the regenerated burst generator and the chroma clamp interval is shortened so that the chroma signal fed to the video output module contains original burst.

PEB and NEB Potentials

The PEB (positive error bus) and NEB (negative error bus) potentials which control the electronically variable video delay line are developed from the phase error signal from the color error detector module utilizing circuitry contained in the color processor module, as shown in figure 8. The phase error signal is an indication of the phase relationship between the reference subcarrier and tape burst signals, and varies linearly as the phase difference between reference subcarrier and tape burst fluctuates. However, the characteristics of the video delay line in the color delay module are such that the delay varies non-linearly in response to a linearly varying d-c potential impressed across it. It is desired that the delay of the video delay line vary linearly; therefore it is necessary to convert the linearly varying phase error signal to a non-linear potential having gain characteristics which match the delay characteristics of the video delay line. The non-linear conversion is accomplished by a differential amplifier circuit incorporating a gamma network containing resistors having values calculated to produce a non-linear output which compensates for the non-linearity of the video delay line.

The non-linear error signal is split in phase, and signals of opposite polarity drive complementary symmetry emitter followers which produce the PEB and NEB potentials. It is important that the PEB and NEB potentials be equal and opposite in polarity, with respect to the delay line reference voltage to which the video signal in the electronically variable video delay line is referred, over the entire phase error signal range; therefore potentiometers are provided as a means of adjusting the PEB and NEB potentials and thereby insuring that a change in NEB potential will be accompanied by an equal and opposite change in PEB potential. Potentiometers are also provided as a means of adjusting the transient behavior of the PEB and NEB potentials so that their rise times will be as nearly equal and opposite as possible in response to a step of error such as occurs at switching when vacuum guide error is present.

The center of the delay range of the video delay line in the color delay module occurs at a PEB

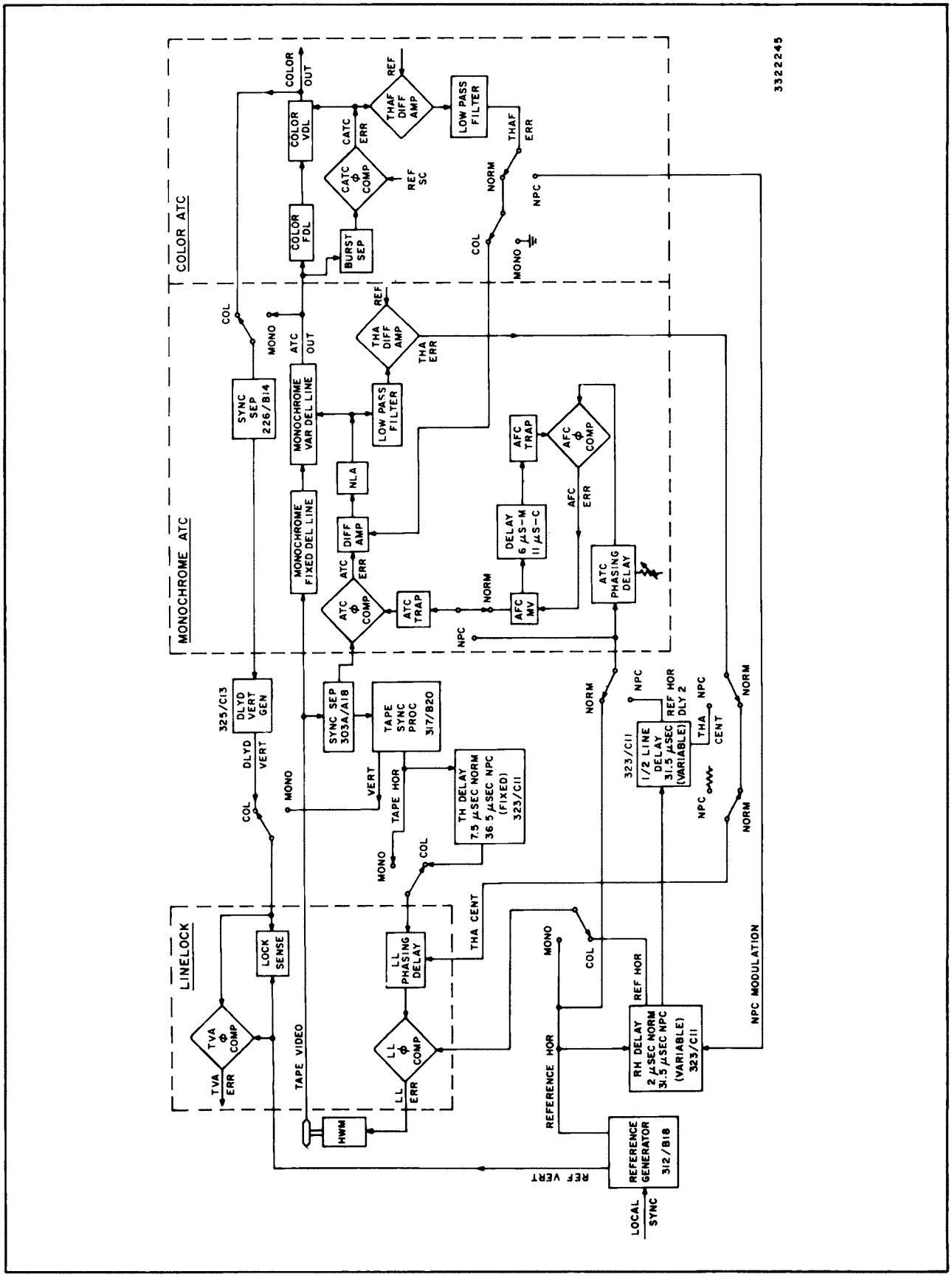


Figure 9—Pixlock Servo with Monochrome and Color ATC

potential of +2.9 volts and a NEB potential of −2.9 volts with respect to the delay line reference potential (nominally −10 volts). Since it is desired that the average PEB and NEB potentials occur at these respective values, an error signal is developed which changes the phase of the tape signal in such a direction as to cause the phase error signal to result in a PEB potential of +2.9 volts with respect to the delay line reference potential. The error signal developed is designated THAF (tape horizontal alignment, fine) and is obtained from a comparison of the PEB potential with a reference voltage, set by means of a potentiometer, in a differential amplifier circuit. The THAF error signal is developed only during color tape playback in the normal color ATC or non-phased color mode. Under any other conditions a clamping circuit in the color error detector module provides a steady potential which corresponds to zero phase error, thereby maintaining a PEB potential of +2.9 volts with respect to the delay line reference potential and therefore a THAF signal of zero. A THAF clamping circuit prevents the THAF error signal from exceeding a certain magnitude in either the positive or negative direction, and thereby minimizes the "cracking effect" described above in the discussion on burst circuits.

THAF Closed Loop System

The color ATC system, basically an open loop servo as is the monochrome ATC system, contains a closed feedback loop to the headwheel servo which is similar in operation to the THA (tape horizontal alignment) loop in the monochrome ATC system. The closed feedback loop in the color ATC system is designated the THAF (tape horizontal alignment, fine) loop.

Figure 9 is a block diagram of the THA and THAF closed feedback loops to the headwheel servo. The block diagram shows only those functions of the headwheel servo, monochrome ATC system, and color ATC system which are within the THA and THAF closed loops, and the switching circuits shown include only those functions which distinguish between operation in the monochrome ATC mode (color off), the normal color ATC mode, or the NPC (non-phased color) mode. The operation of the THA loop in the monochrome ATC mode has been discussed in detail in the *Monochrome ATC* instruction book (IB-31661). In general, however, the principal function of the THA loop is to automatically adjust the phase of the headwheel servo to maintain the average sampling of the monochrome ATC in the center of its error detector slope, which in turn has been set by internal adjustments to correspond to the PEB (positive error bus) potential representing the center delay of the monochrome variable delay line.

Normal Color ATC Mode

The principal function of the THAF loop in the color ATC system, during playback in the normal color ATC mode, is to automatically adjust the phase of the monochrome ATC output signal to maintain the average sampling of the color ATC in the center of its error detector slope. The center of the error detector slope in the THAF loop has also been set up by internal adjustment to correspond to the PEB voltage representing the center delay of the color variable delay line. The actual operation is accomplished in several steps. First, the THAF error signal is generated by comparing the PEB potential to a reference voltage. The resulting error signal is applied, through a low pass filter, to the reference side of the input differential amplifier in the monochrome non-linear amplifier circuit. (See figure 9.) Therefore a change in THAF error signal will generate a change in the potential of the monochrome ATC error busses (PEB, NEB, DPEB, and DNEB) which are applied to the monochrome variable delay line. The change in error bus potential in turn causes the delay of the monochrome variable delay line to change in such a direction as to correct the average phase of the signal applied to the color ATC system.

In correcting the average phase of the signal applied to the color ATC system, the average delay of the monochrome variable delay line will shift from its nominal center value corresponding to a PEB potential of +2.9 volts. The THA differential amplifier in the monochrome ATC system will measure this change in PEB potential and generate its own error signal which feeds back to the phasing delay in the linelock module. A change in the linelock phasing delay in turn causes the headwheel to advance or retard so that the monochrome variable delay line is restored to operation in the center of its delay range.

The net result of the closed loop servo action during playback in the normal color ATC mode is that the headwheel is changed in phase to supply the correction demanded by the color ATC system, and the monochrome variable delay line is still operating in the center of its delay range but the monochrome ATC error detector is shifted slightly from operation in the center of its slope. It should be noted that the bandwidth of the THAF loop is somewhat greater than that of the THA loop. Therefore, changes in the average THAF voltage occurring at a frequency

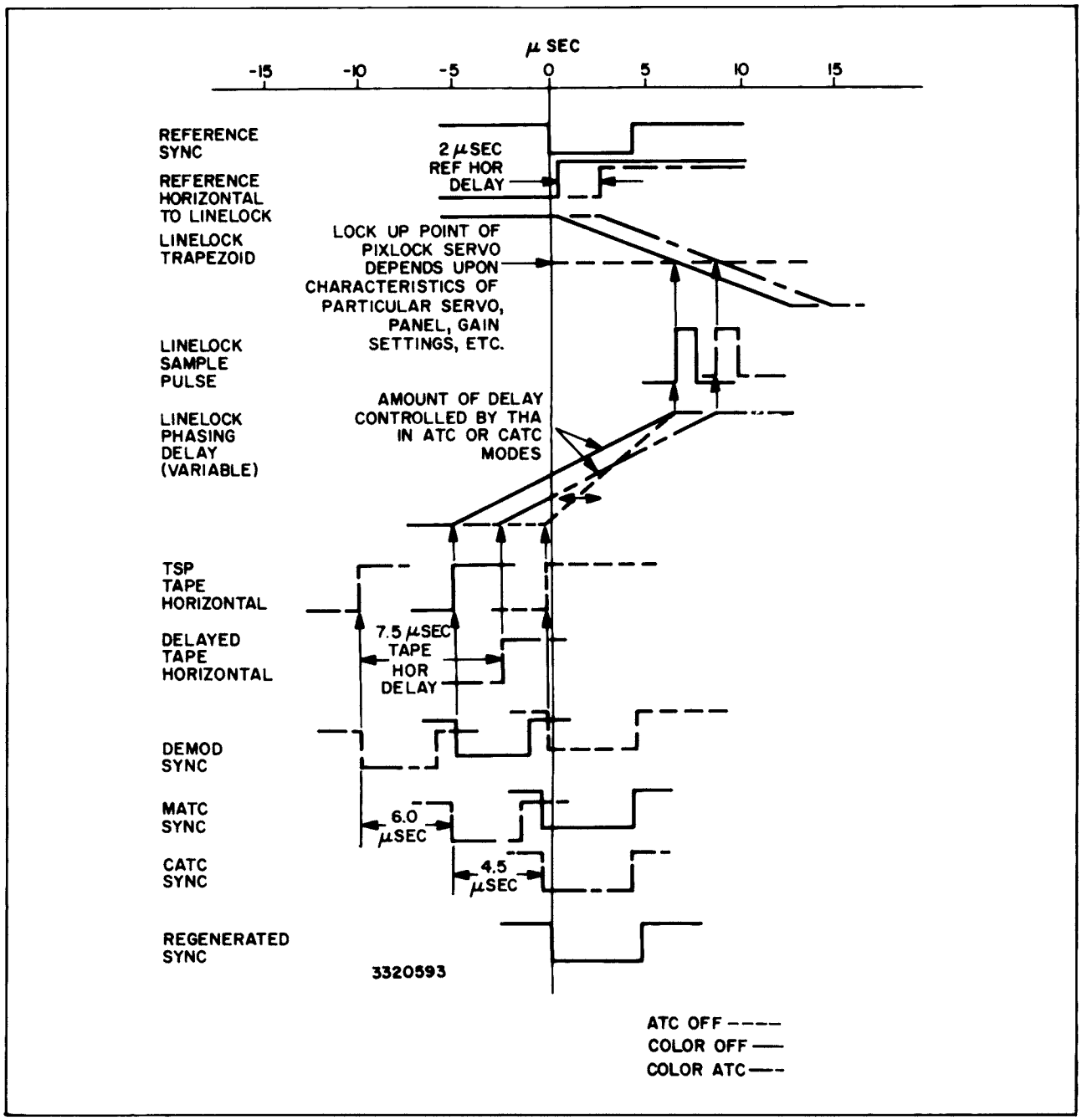


Figure 10—Pixlock Servo System Horizontal Timing Relationships During Color Tape Playback in the Normal Color ATC Mode

greater than the THA loop bandwidth will be corrected by changing the delay of the monochrome variable delay line rather than by changing the phase of the headwheel.

There are several fixed delays shown in figure 9 which are not basic to the operation of the THAF loop during playback in the normal color ATC mode. The 7.5 microsecond tape horizontal delay and the 2 microsecond reference horizontal delay are inserted into the tape horizontal and reference horizontal paths respectively. The net difference in the two delays represents a 5.5 microsecond delay in series with the linelock phasing delay. The purpose of this net delay is to maintain the operation of the variable linelock phasing delay at nominally the same delay time during playback in the normal color ATC mode as it is during playback in the monochrome ATC

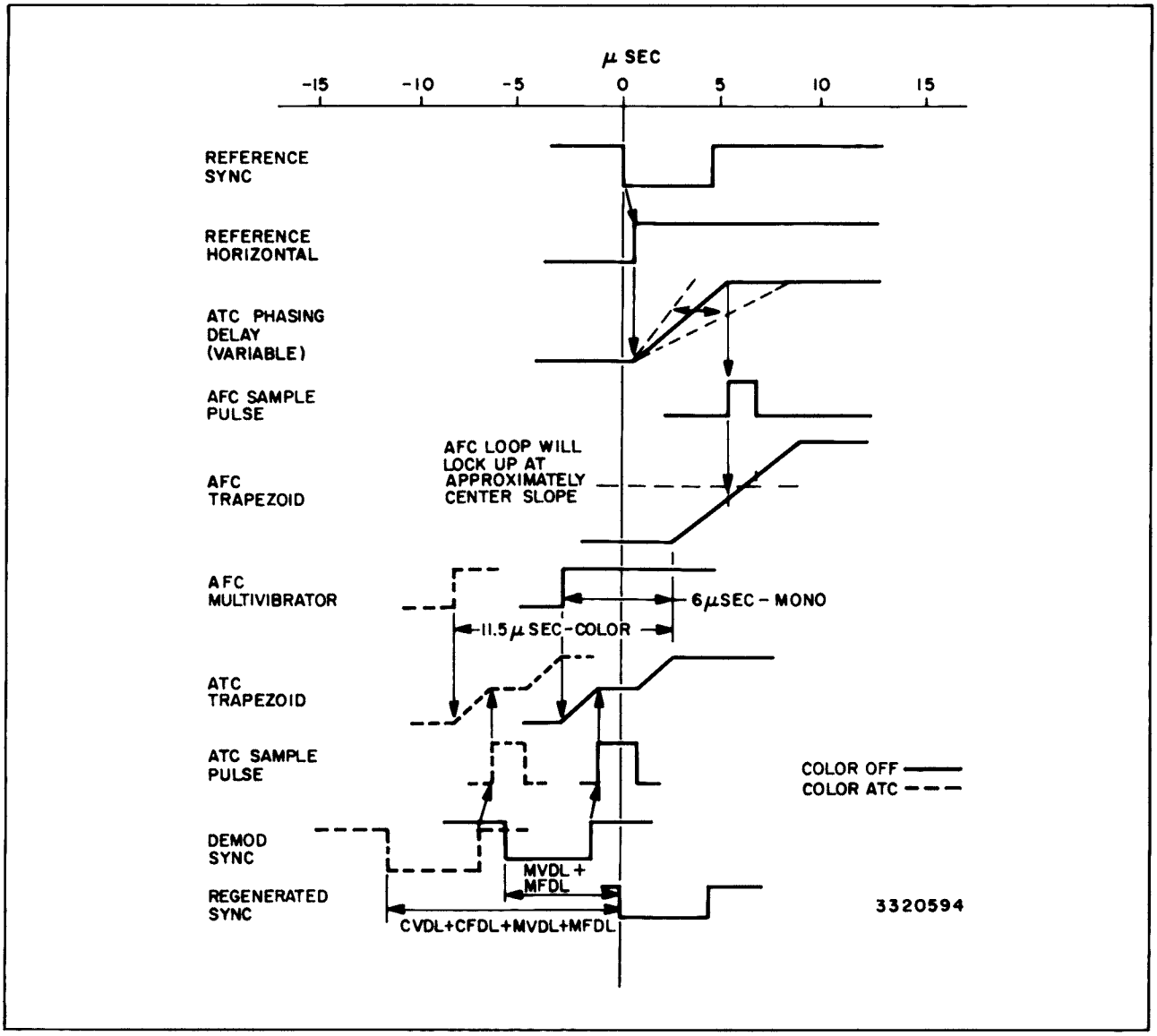


Figure 11—Monochrome ATC System Horizontal Timing Relationships During Color Tape Playback in the Normal Color ATC Mode

(color off) mode, while at the same time increasing the total delay to that value which will advance the headwheel by an amount equivalent to the delay inserted into the signal path by the color fixed delay line and the color variable delay line. (The timing relationship of the horizontal signals utilized in the pixlock servo system and in the monochrome ATC system during color tape playback in the normal color ATC mode are shown in the timing diagrams, figures 10 and 11.)

A fixed delay is also inserted into the path of the tape vertical signal applied to the TVA (tape vertical alignment) and lock sense circuits of the linelock module. If the output signal from the machine is to be aligned with reference sync (as it normally is), the output from the demodulator must be advanced considerably because of the delays presented by the monochrome fixed and variable delay lines and the color fixed and variable delay lines. When the output from the demodulator is advanced, the vertical output from the demodulator is no longer in coincidence with reference vertical and may actually be advanced sufficiently to cause the vertical coincidence circuit to drop out when locking up in color playback and thereby throw the servo out of the pixlock mode. Therefore, to prevent the machine from falling out of the pixlock servo mode during color tape playback, tape vertical is timed to the output signal by the fixed delay inserted into the tape vertical path.

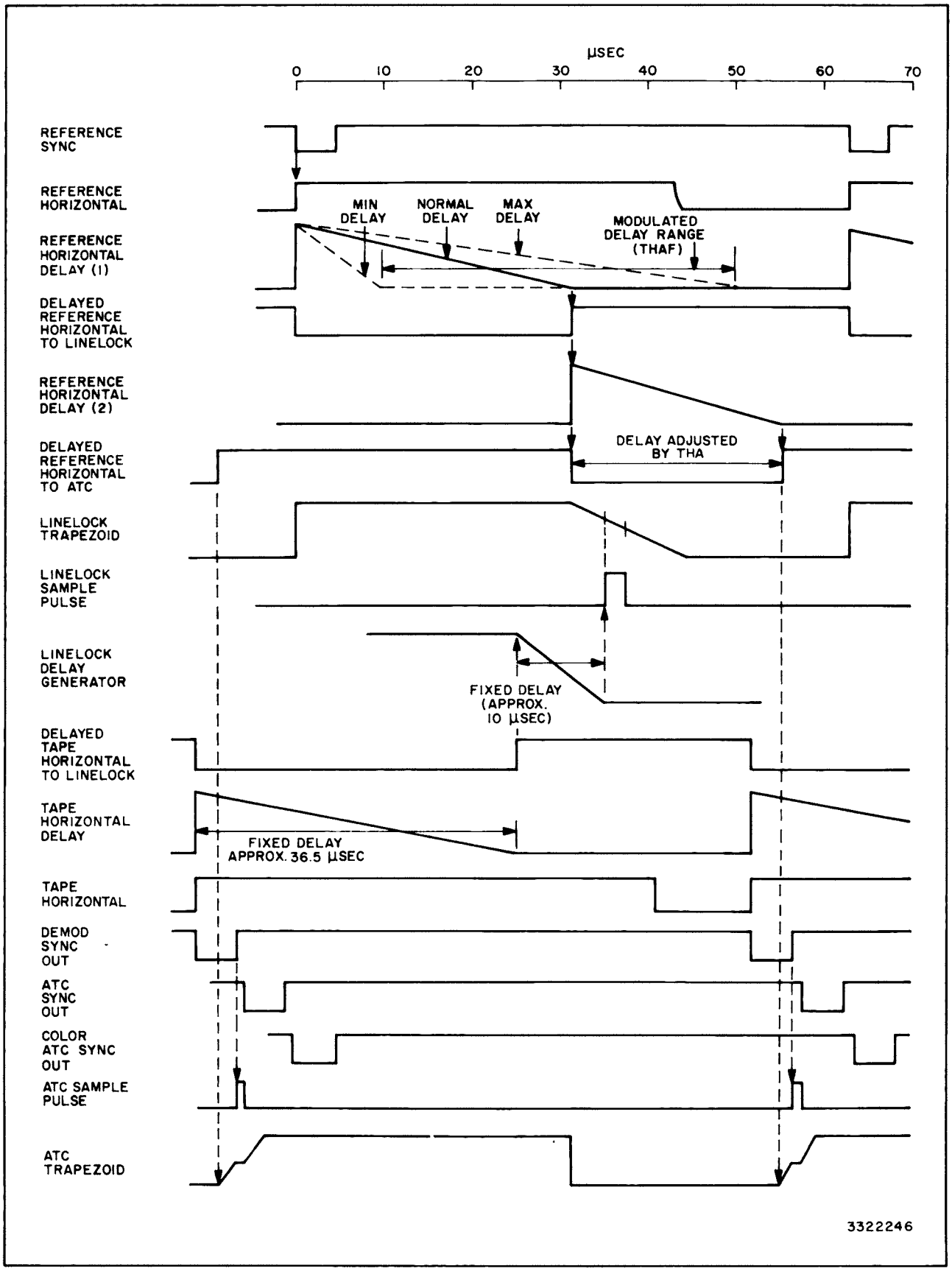


Figure 12—Horizontal Timing Relationships During Color Tape Playback in the NPC Mode

NPC (Non-Phased Color) Mode

In the NPC mode of color tape playback the requirements are somewhat different than in the normal color ATC mode. The principal function of the NPC mode is to allow playback of non-interlaced color (NIC) tapes. Non-interlaced color tapes are produced by dubbing a playback from a heterodyne color system. Inherent in the heterodyne color system is an output signal in which the phases of the monochrome and chroma portions of the signal are displaced by an amount which is equal to the jitter of the tonewheel servo of the machine making the original recording and thus no longer bear a fixed relationship to each other. Therefore, the linelock and the monochrome ATC circuits, which are attempting to time-base correct the video signal by comparing tape sync to reference sync, and the color ATC system, which is attempting to time-base correct the video signal by comparing tape burst to reference subcarrier are apparently presenting conflicting information. However, the presentation of conflicting information is avoided by causing the color ATC system to assume control.

As the relative phase between tape burst and reference subcarrier attempts to change, the THAF differential amplifier senses this and generates a signal which modulates a delay in the path of reference sync fed to the linelock and monochrome ATC circuits. The headwheel servo and monochrome ATC systems will follow this change in phase of reference sync in such a manner that the phase of tape burst does not change with respect to that of the reference subcarrier. The bandwidth of the THAF loop during color tape playback in the NPC mode must be greater than that of the tonewheel servo which generated the original tape. The net result is that the output signal from the machine will vary in phase in such a manner that the chroma signal bears a fixed phase relationship to reference subcarrier. I.e., the output signal will be non-interlaced color, but will be as satisfactory as the original non-interlaced color playback.

To accomplish modulation of the reference horizontal delay with as great a range as possible, it is necessary to provide a nominal delay of approximately one-half a TV line. The nominal delay may then be modulated ± 20 microseconds, if necessary, to follow the jitter of a very loose servo. (Refer to the NPC horizontal timing diagram, figure 12.) A similar fixed delay of approximately one-half a TV line is inserted into the tape horizontal path so that the undelayed tape signal retains approximately the same phase relationship to the undelayed reference sync during playback in the NPC mode that it does during playback in the normal color ATC mode. This allows the headwheel servo to operate in the pixlock mode during color tape playback in the NPC mode since vertical alignment is maintained.

Even though the tape signal is varying in time in response to modulation of the reference horizontal delay, if its nominal position is centered with respect to reference vertical the excursions will not exceed the range of the lock sense circuit. In tape recorders equipped for the linelock only (LLO) servo mode, it is advantageous to operate in that mode during NPC playback where vertical coincidence is not required. Since the exact horizontal phasing is not predictable when playing back a non-interlaced color tape (nor is it precisely adjustable when playing back an interlaced color tape in the NPC mode), there is no possibility of mixing, fading, or incorporating special effects, etc. The prime purpose of the normal color ATC mode is to provide these possibilities during playback in the pixlock servo mode.

Delayed reference horizontal with the same modulation must also be fed to the monochrome ATC system. (If the monochrome ATC system were operating from fixed horizontal reference, it would attempt to correct the timing modulation which has been inserted into the tape signal by the headwheel servo.) However, the delayed reference horizontal is delayed by nominally one-half a TV line, whereas the tape signal is nominally aligned to undelayed reference horizontal. Therefore, it is necessary to insert another half-line delay in the reference horizontal path to the monochrome ATC system to insure that the monochrome ATC trapezoid waveform is properly timed so that the sample pulse will fall on its slope. This nominal half-line delay is automatically adjusted to be precisely the correct amount to cause average sampling at the center of its slope by the THA error signal. It should be noted that the THA loop is relatively limited in bandwidth so that the ATC is still performing its normal function of removing timing errors such as quadrature, jogs, etc. It should also be noted that the THAF loop during NPC playback is also bandwidth limited, so that it does not respond to the normal line-by-line correction of phasing errors by the color ATC system.

There is one further refinement of monochrome ATC operation required for color tape playback in the NPC mode. This refinement consists of bypassing the AFC loop to form the ATC trapezoid directly from the delayed reference horizontal. The AFC loop performs no useful function in the external mode of monochrome ATC operation and is actually detrimental during color tape playback in the NPC mode

because it provides undesired bandwidth limiting and an additional phase shift which makes the high gain THAF loop very difficult to stabilize. During color tape playback in the normal color ATC mode, however, the AFC loop provides a required timing advance which is not required during NPC operation because a delay of one full TV line is provided.

Control and Indicator System

Installation of the monochrome ATC system includes all external relays, wiring, and indicators required for color ATC operation. The monochrome ATC control and indicator system is described in the monochrome ATC instruction book (IB-31661), and only those control and indicator circuits which pertain to color tape playback in the normal color ATC or non-phased color (NPC) mode will be described in this instruction book. Applicable diagrams include the monochrome ATC and color ATC system functional diagrams for TR-22 and TR-3/TR-4 machines and the ATC control system functional diagrams for TR-22 and TR-3/TR-4 machines, figures 78 through 83, located at the rear of this instruction book.

The color ATC control and indicator circuits contain both external and internal relays. In TR-22 machines the external relays are mounted on the ATC relay bank located at the rear of the machine. In TR-3/TR-4 machines the external relays are contained in the ATC relay module (no. 3A1) located behind the control panel. The external relay numerical designations in TR-22 machines are preceded by the number 11 (e.g., 11K21, 11K22, etc.) which identifies their location in the machine. To avoid confusion in the following relay functional descriptions, the external relays are referred to simply as K21, K22, etc. and their functions pertain to TR-22, TR-3, and TR-4 machines. The internal relays are those contained within the monochrome ATC reference module and the color processor module.

Color ATC Bypass System

The color ATC system contains four color bypass relays, which are designated K21, K22, K23, and K24. (See figures 78 through 83.) One side of the coils of these relays is connected to the −26 volt dc supply. The other side of the coils is connected through the color ATC module interlock system to an 'AND' gate circuit in the color phase module (no. 232/C16). The inputs to the 'AND' gate are (1) the ATC mode control from function selector switch S1 on the ATC delay/output module (no. 223/B11) and (2) the output from a second 'AND' gate in the color phase module. The ATC mode control is ground when the function selector switch on the ATC delay/output module is in either COLOR ATC or NON-PHASED COLOR position. When the function selector switch is in either COLOR OFF or ATC OFF position the ATC mode control is an open circuit. The second 'AND' gate in the color phase module is controlled by (1) the monochrome ATC interlock control and (2) the output from an 'OR' gate, also in the color phase module circuitry. The monochrome ATC interlock control is ground when all monochrome ATC modules are securely in place and the function selector switch on the ATC delay/output module is in COLOR OFF, COLOR ATC, or NON-PHASED COLOR position. Under any other conditions the ATC interlock control is an open circuit. The output from the 'OR' gate is ground when selector switch S1 on the FM standards module (no 205) in TR-22 machines is in COL-1 or COL-2 position or; when selector switch S1 on the demodulator output module (no. A18) in TR-3/TR-4 machines is in COL position. If these switches are in any other position, the 'OR' gate will not produce a ground potential. When the output from the 'OR' gate and the ATC interlock control are both ground, the output from the second 'AND' gate in the color phase module is also ground. When the output from the second 'AND' gate and the ATC mode control are both ground, the output from the first 'AND' gate is also ground. Then, when the output from the first 'AND' gate is ground and all color ATC modules are securely in place, ground is applied to the coils of the color bypass relays and they are energized (i.e., in the COLOR mode). Table II sums up the conditions which must exist in order to energize the color bypass relays during color tape playback. If any of these conditions are not met, all color bypass relays will be deenergized (i.e., in the BYPASS mode).

Each of the color bypass relays has two sets of two-way contacts, A and B. When the relays are energized they perform the following functions:

> NOTE: When the conditions exist which cause the color bypass relays to be energized, the monochrome bypass relays are also energized (i.e., in the MONO mode).

1. Contact A of relay K21 connects the low pass output from the chroma separator module (no. 325/C13) to the sync separator circuit in the monochrome ATC reference module (no. 226/B14) and to video processing circuits in the video control module (no. 131/A21), via monochrome bypass relay K11A.

2. Contact B of relay K21 supplies ground potential to the AFC delay circuit in the ATC reference module.

TABLE II — CONDITIONS REQUIRED TO ENERGIZE COLOR BYPASS RELAYS DURING COLOR TAPE PLAYBACK

TR-22 Machines	All monochrome ATC and color ATC modules securely in place. Selector switch on ATC delay/output module (no. 223) in COLOR ATC or NON-PHASED COLOR position. Selector switch on FM standards module (no. 205) in COL-1 or COL-2 position.
TR-3/TR-4 Machines	All monochrome ATC and color ATC modules securely in place. Selector switch on ATC delay/output module (no. B11) in COLOR ATC or NON-PHASED COLOR position. Selector switch on demodulator output module (no. A18) in COL position.

3. Contact A of relay K22 connects delayed reference horizontal from the color sensor module (no. 323/C11) to the linelock trapezoid generator in the linelock module (no. 316/B19).

4. Contact B of relay K22 connects delayed tape horizontal from the color sensor module to the linelock sample pulse generator in the linelock module.

5. Contact A of relay K23 connects delayed tape vertical from the chroma separator module to the lock sense circuit in the linelock module.

6. Contact B of relay K23 connects the THAF signal from the color processor module (no. 231/C15) to the THAF differential amplifier in the monochrome error detector module (no. 225/B13) via NPC relay K31B when the machine is playing back color tape in the normal color ATC mode. (When the machine is playing back color tape in the NPC mode, contact B of relay K23 is connected to an open circuit.)

7. Contact A of relay K24 grounds the NPC bus through contact A of relay K41 when the mode selector switch on the ATC delay/output module is in NON-PHASED COLOR position and the machine is in the pixlock servo mode. This action energizes external NPC relays K31 and K32, energizes internal relay K1 in the monochrome ATC reference module, energizes internal relay K2 in the color processor module, and applies ground potential to the switchable current source circuit in the color sensor module.

In addition, in TR-22 machines contact A of relay K24 supplies ground potential to the NON-PHSD COLOR indicator (5DS16), located above the tape transport panel, when the mode selector switch on the ATC delay/output module is in NON-PHASED COLOR position, thereby causing the indicator to light and thus signify color tape playback in the NPC mode.

8. Contact B of relay K24 supplies ground potential to the COLOR ATC indicator (5DS15), located above the tape transport panel on TR-22 machines, when the mode selector switch on the ATC delay/output module is in COLOR ATC position, thereby causing the indicator to light and thus signify color tape playback in the normal color ATC mode. (In TR-3/TR-4 machines contact B of relay K24 is not used.)

When the color bypass relays are deenergized (i.e., in the BYPASS mode), and the monochrome bypass relays are energized (MONO mode), the color bypass relays perform the following functions:

1. Contact A of relay K21 disconnects the low-pass signal from the monochrome ATC reference and video control modules, and connects the monochrome ATC video signal from the monochrome ATC delay/output module to the sync separator circuit in the monochrome ATC reference module and to video processing circuits in the video control module, via monochrome bypass relay K11A.

2. Contact B of relay K21 disconnects the ground potential to the AFC delay circuit in the ATC reference module.

3. Contact A of relay K22 disconnects delayed reference horizontal from the linelock module, and connects undelayed reference horizontal from the reference generator module (via the color sensor module) to the linelock trapezoid generator in the linelock module and to the monochrome ATC reference module via NPC relay K31A when playing back a color tape in the normal color ATC mode.

4. Contact B of relay K22 disconnects delayed tape horizontal from the linelock module, and connects undelayed tape horizontal from the tape sync processor module, no. 317/B20, (via the color sensor module) to the linelock sample pulse generator in the linelock module.

5. Contact A of relay K23 disconnects delayed tape vertical from the linelock module, and connects undelayed tape vertical from the tape sync processor module (via the chroma separator module) to the lock sense circuit in the linelock module.

6. Contact B of relay K23 disconnects the THAF signal from the monochrome error detector module, when the machine is playing back color tape in the normal color ATC mode, and returns the THAF signal to ground.

7. Contact A of relay K24 removes ground potential from the NON-PHSD COLOR indicator and from the NPC bus.

8. Contact B of relay K24 removes ground potential from the COLOR ATC indicator.

NPC Control System

The NPC (non-phased color) control system contains two external NPC relays (K31 and K32), and two internal NPC relays (K1 in the monochrome ATC reference module, no. 226/B14, and K2 in the color processor module, no. 231/C15). (See figures 78 through 83.) One side of the coils of these relays is connected to the −26 volt dc supply. The other side of the coils is connected to the NPC bus. The NPC bus is at ground potential when the selector switch on the monochrome ATC delay/output module is in NON-PHASED COLOR position and the machine is in the pixlock servo mode. When the NPC bus is grounded, the NPC relays are energized (i.e., in the NPC mode).

Each of the NPC relays has two sets of two-way contacts, A and B. When the relays are energized they perform the following functions:

1. Contact A of relay K31 connects delayed reference horizontal from the color sensor module to the monochrome ATC reference module where it is utilized in generating the monochrome ATC trapezoid waveform (via internal relay K1A).

2. Contact B of relay K31 connects the THAF output signal from the color processor module to the reference horizontal delay circuit in the color sensor module.

3. Contact A of relay K32 connects a steady d-c voltage from the color sensor module to the linelock sample pulse delay control circuit in the linelock module.

4. Contact B of relay K32 connects the THA signal from the monochrome ATC reference module to the reference horizontal variable delay circuit in the color sensor module when the monochrome ATC system is operating in EXTERNAL mode.

5. Contact A of relay K1 in the monochrome ATC reference module connects delayed reference horizontal to the monochrome ATC trapezoid generator.

6. Contacts A and B of relay K2 in the color processor module switch in the larger capacitance in the time constant circuit of the THAF differential amplifier.

When the NPC relays are deenergized (i.e., in the NORM mode), the relays perform the following functions:

1. Contact A of relay K31 disconnects delayed reference horizontal from the monochrome ATC reference module and connects undelayed reference horizontal from the reference generator module (via the color sensor module) to the ATC reference module where it is utilized in generating the AFC sample pulse when the monochrome ATC system is operating in the EXTERNAL mode.

2. Contact B of relay K31 disconnects the THAF signal from the color sensor module and connects the signal to the differential amplifier circuit in the monochrome error detector module.

3. Contact A of relay K32 disconnects the constant d-c voltage from the linelock sample pulse delay control circuit in the linelock module and, in conjunction with contact B of relay K32, connects the THA signal from the monochrome ATC reference module to the delay control circuit in the linelock module.

4. Contact B of relay K32 disconnects the THA signal from the delayed reference horizontal circuit in the color sensor module and, in conjunction with section A of relay K32, connects the THA signal from the monochrome ATC reference module to the linelock sample pulse delay control circuit in the linelock module.

5. Contact A of relay K1 in the monochrome ATC reference module disconnects delayed reference horizontal from the monochrome ATC trapezoid generator and connects the horizontal oscillator output to the trapezoid generator.

6. Contacts A and B of relay K2 in the color processor module switch out the larger capacitance in the time constant circuit of the THAF differential amplifier and switch in the smaller capacitance.

Tonewheel/Pixlock Mode Control System

The tonewheel/pixlock mode control system contains relay K41. (See figures 82 and 83.) One side of the coil of relay K41 is connected to the −26 volt dc supply. The other side of the relay coil is connected to the PL (pixlock) position of the servo mode selector switch on the tape sync processor module (no. 317/B20). When the selector switch is in PL position and the machine is operating in the PLAY mode, ground potential is applied to the pixlock bus and thus to the coil of relay K41. Relay K41 is thereby energized and is inserted in series with relay K24A, thus allowing ground potential to be applied to the NPC bus when the selector switch on the monochrome ATC delay/output module is in NON-PHASED COLOR position.

> NOTE: In machines which have the "linelock only" facility, relay K41 is energized when the servo mode selector switch is in either "pixlock" or "linelock" position.

The LOCK bus, which is at ground potential when the headwheel servo has achieved a "lock" in the pixlock or linelock servo mode, is also utilized in the monochrome and color ATC control systems. In the monochrome ATC system it energizes the INT/EXT relays in the monochrome ATC reference module (no. 226/B14). In the color ATC system it is required in the generation of new burst and in the suppression of old burst in the color processor module (no. 231/C15), and to unclamp the color error detector in the color error detector module (no. 326/C14).

Color Processor Module Control Circuits

Circuits within the color processor module (no. 231/C15) which are controlled wholly or in part by the color ATC system operating conditions include an 'AND' gate circuit and two relay circuits (K1 and K2). (See figures 82 and 83.) The relationship of these circuits to the remainder of the color ATC system is described below. For a detailed description of the circuit operations refer to the color processor module circuit description.

The 'AND' gate in the color processor module controls the regenerated burst killer circuit and a monostable multivibrator in the THAF clamping circuit. The 'AND' gate produces a ground potential output which allows these circuits to operate normally when three conditions exist. These conditions are (1) the color interlock control bus must be ground, (2) the pixlock sense bus must be ground, and (3) the burst sensor control potential, from the color sensor module, must be ground. The first condition listed above is controlled by the color ATC system operating conditions. These conditions in turn are (1) the monochrome ATC and color ATC modules must be securely in place, (2) the function selector switch on the monochrome ATC delay/output module (no. 223/B11) must be in either COLOR ATC or NON-PHASED COLOR position, and (3) in TR-22 machines the selector switch on the FM standards module (no. 205) must be in COL-1 or COL-2 position, or, in TR-3/TR-4 machines the selector switch on the demodulator output module (no. A18) must be in COL position.

Relay K1 controls the chroma output from the color processor module. When the relay is energized, chroma is fed to the video output module. The relay is energized when the color interlock control bus is ground, and the conditions required for grounding the control bus are listed in the above paragraph.

Relay K2 controls the THAF differential amplifier low-pass filter in the chroma processor module. The value of the low-pass filter changes according to whether the machine is playing back a color tape in the normal color ATC or non-phased color mode. When the machine is operating in the normal color ATC mode the NPC bus is essentially an open circuit and relay K2 is deenergized. When the machine is operating in the NPC mode the NPC bus is at ground potential and relay K2 is energized.

Color Phase Module Control Circuits

Circuits within the color phase module (no. 232/C16) which are controlled by the color ATC system operating conditions include two 'AND' gates and, in TR-22 machines, an 'OR' gate. The 'AND' gates and the 'OR' gate combine to provide a ground potential on the color interlock control bus when the required color ATC system conditions are met. These conditions are (1) the monochrome ATC and color ATC modules must be securely in place, (2) the function selector switch on the monochrome ATC

delay output module (no. 223/B11) must be in either COLOR ATC or NON-PHASED COLOR position, and (3) in TR-22 machines the selector switch on the FM standards module (no. 205) must be in COL-1 or COL-2 position, or, in TR-3/TR-4 machines the selector switch on the demodulator output module (no. A18) must be in COL position.

Indicator Circuits (TR-22 Machines Only)

Three indicator lights are utilized with the color ATC system. (See figure 82.) These are the COLOR ATC, NON-PHSD COLOR, and COLOR STD indicators, all located in the row of indicators above the tape transport panel and PLAY control panel. The COLOR ATC and NON-PHSD COLOR indicators identify the mode of color tape playback. When the machine is playing back a color tape in the normal color ATC mode, color bypass relay K24B is energized and the COLOR ATC indicator is illuminated by a ground from the switch. When the machine is playing back a color tape in the NPC (non-phased color) mode, relay K24A is energized and the NON-PHSD COLOR indicator is illuminated. The COLOR STD indicator identifies the post-emphasis network in the FM standards module (no. 205). The COL-1 and COL-2 positions of the post-emphasis selector switch on the FM standards module are tied together in the module; therefore, when the switch is in either COL-1 or COL-2 position the COLOR STD indicator is illuminated.

NOTE: Although not an integral part of the color ATC control system, the LOCK portion of the pix-lock servo mode indicator must also be illuminated during color tape playback. This signifies that the machine is "locked" in the pixlock servo mode, as required for color ATC operation.

SYSTEM ADJUSTMENTS

The color ATC system has been adjusted for domestic (3.58 mc subcarrier) operation at the factory prior to shipment. However, after the system has been installed it is advisable to make the setup adjustments presented below to insure that video, chroma, and burst levels are correct for the particular installation. Additional adjustments which are required for operation on the proposed International standard (625-line/50 cps; 4.43 mc subcarrier) are included at the end of the *Setup Adjustments* section. Machine setup and video level adjustment procedures are presented for each series machine (TR-22, TR-4, and TR-3 machines respectively), and the remaining setup adjustments apply to all series machines unless otherwise specified.

A section on maintenance adjustment procedures follows the system *Setup Adjustments* section. The maintenance adjustment procedures are normally required only when the controls have been inadvertently misadjusted or when necessitated by component replacement, and are applicable to all series machines.

Both adjustment sections include procedures which require a vacuum-tube voltmeter such as the *RCA Type WV-98A VoltOhmyst,* or the equivalent, and a dual-trace oscilloscope such as the *Tektronix Type 535-A,* or the equivalent. Before proceeding with the adjustments, verify that 1 volt peak-to-peak on the external oscilloscope corresponds to 1 volt peak-to-peak (140 IRE units) on the machine CRO monitor (TR-22 and TR-4 machines).

SETUP ADJUSTMENTS

TR-22 Machine Setup

Set up TR-22 machines in the following manner when making system adjustments:

1. Rotate the selector switch on the FM standards module (no. 205) to COLOR STD 1 or 2 position.

2. Rotate the mode selector switch on the monochrome ATC delay/output module (no. 223) to COLOR ATC or NON-PHASED COLOR position.

3a. For back-to-back (MOD-DEMOD) operation, feed a color bar signal (split field with 100% white bar), 3.58 mc subcarrier, and sync to the machine, and operate the machine in STOP (MOD-DEMOD) mode.

NOTE: For International operation, feed the 625-line/50-cycle field CCIR standard video, sync, and 4.43 mc subcarrier signals to the machine.

3b. To play back a color test tape, feed a 3.58 mc subcarrier (4.43 mc subcarrier if the machine is operating on 625-line standards) and sync to the machine, and play back a tape containing a color bar signal (split field with 100% white bar) in the pixlock (or linelock) servo mode.

TR-4 Machine Setup

Set up TR-4 machines in the following manner when making system adjustments:

1. Rotate the selector switch on the demodulator output module (no. A18) and the selector switch on the modulator module (no. A2) to COLOR position.

2. Rotate the mode selector switch on the monochrome ATC delay/output module (no. B11) to COLOR ATC or NON-PHASED COLOR position.

3a. For back-to-back (MOD-DEMOD) operation, feed a color bar signal (split field with 100% white bar), 3.58 mc subcarrier, and sync to the machine, and operate the machine in STOP (MOD-DEMOD) mode.

NOTE: For International operation, feed the 625-line/50-cycle field CCIR standard video, sync, and 4.43 mc subcarrier signals to the machine.

3b. To play back a color test tape, feed a 3.58 mc subcarrier (4.43 mc subcarrier if the machine is operating on 625-line standards) and sync to the machine, and play back a tape containing a color bar signal (split field with 100% white bar) in the pixlock (or linelock) servo mode.

TR-3 Machine Setup

Set up TR-3 machines in the following manner when making system adjustments:

1. Rotate the selector switch on the demodulator output module (no. A18) to COLOR position.

2. Rotate the mode selector switch on the monochrome ATC delay/output module (no. B11) to COLOR ATC or NON-PHASED COLOR position.

3a. For simulated back-to-back operation, remove the video out pins (nos. 14 and 30) from the demodulator output module receptacle at the rear of the machine, feed a 1 volt peak-to-peak (140 IRE unit) video signal to the pins (white bar should be 100 IRE units), feed 3.58 mc subcarrier and sync signals to the machine, and operate the machine in STOP mode.

NOTE: For International operation, feed the 625-line/50-cycle field CCIR standard video, sync, and 4.43 mc subcarrier signals to the machine.

3b. To play back a color test tape, feed a 3.58 mc subcarrier (4.43 mc subcarrier if the machine is operating on 625-line standards) and sync to the machine, and play back a tape containing a color bar signal (split field with 100% white bar) in the pixlock (or linelock) servo mode.

TR-22 Machine Video Level

1. Set up the machine for back-to-back (MOD-DEMOD) operation as instructed in the *TR-22 Machine Setup* procedure at the beginning of this section, except that in step 2 rotate the mode selector switch on the monochrome ATC delay/output module to ATC OFF position.

2. Depress the VID IN pushbutton on the CRO monitor switcher and adjust the LEVEL control on the video input module (no. 103) for a 1 volt peak-to-peak (140 IRE unit) video signal. (White bar should be 100 IRE units.)

3. Depress the DEMOD OUT pushbutton on the CRO monitor switcher, set the carrier frequency and deviation according to normal procedure, and adjust DEMOD LEVEL screwdriver control on the FM standards module (no. 205) for 100 IRE units white bar.

4. Place the video control module (no. 131) on a module extender, and connect one probe of the external oscilloscope to the VID IN test point on the video control module front panel and connect the other probe of the external oscilloscope to the VID 1 test point on the video output module (no. 233) front panel.

5. Adjust the LEVEL control on the video control module for a signal amplitude of approximately 1 volt peak-to-peak at the IN test point.

6. Adjust potentiometer R48 (video control module internal GAIN control) so that the white bar amplitude at the IN test point is equal to that at the VID 1 test point on the video output module. (Reduce the horizontal blanking width temporarily, utilizing the HOR BLKG WIDTH screwdriver control on the sync logic module, no. 230, in order to compare original black to white level without the effect of a new pedestal.)

7. Depress the VID OUT pushbutton on the CRO monitor switcher and observe the CRO monitor while performing steps 8 and 9 below.

8. Adjust the SYNC control on the FM equalizer module (no. 132) to obtain a sync amplitude of 40 IRE units.

9. Adjust the PED control on the video control module for 7.5 IRE units pedestal, and adjust the LEVEL control for 100 IRE units white bar.

10. Re-insert the video control module into its receptacle and place the monochrome ATC delay/output module (no. 223) on the module extender.

11. Connect one probe of the external oscilloscope to the VID 1 test point on the demodulator output module (no. 303) front panel, and connect the other probe to the VID OUT 2 test point on the ATC delay/output module front panel.

12. Adjust potentiometer R3 (ATC delay/output module internal ATC LEVEL control) so that the white bar amplitude at the VID OUT 2 test point is equal to that at the VID 1 test point on the demodulator output module.

13. Re-insert the ATC delay/output module into its receptacle and place the color delay module (no. 324) on the module extender.

14. With one probe of the external oscilloscope remaining at the VID 1 test point on the demodulator output module, connect the other probe to the OUT test point on the color delay module front panel.

15. Adjust potentiometer R13 (color delay module internal COLOR ATC LEVEL control) so that the white bar amplitude at the OUT test point is equal to that at the VID 1 test point on the demodulator output module.

16. Rotate the mode selector switch on the ATC delay/output module to COLOR ATC or NON-PHASED COLOR position.

17. Re-insert the color delay module into its receptacle and place the chroma separator module (no. 325) on the module extender.

18. With one probe of the external oscilloscope remaining at the VID 1 test point on the demodulator output module, connect the other probe to the VID 1 test point on the video output module front panel.

19. Adjust potentiometer R3 (chroma separator module internal COLOR OUTPUT LEVEL control) so that the white bar amplitude at the VID 1 test point on the demodulator output module is equal to that at the VID 1 test point on the video output module.

20. Re-insert the chroma separator module into its receptacle.

TR-4 Machine Video Level

1. Set up the machine for back-to-back (MOD-DEMOD) operation as instructed in the *TR-4 Machine Setup* procedure at the beginning of this section, except that in step 2 rotate the mode selector switch on the monochrome ATC delay/output module (no. B11) to ATC OFF position.

2. Depress the VID IN pushbutton on the CRO monitor switcher and adjust the VIDEO LEVEL control on the video input module (no. A1) for a 1 volt peak-to-peak (140 IRE unit) video signal. (White bar should be 100 IRE units.)

3. Depress the DEMOD OUT pushbutton on the CRO monitor switcher, set carrier frequency and deviation according to normal procedure, and adjust DEMOD LEVEL screwdriver control on the demodulator output module (no. A18) for 100 IRE units white bar.

4. Place the video/FM control module (no. A21) on a module extender, and connect one probe of the external oscilloscope to the VID IN test point on the video control module front panel and connect the other probe of the external oscilloscope to the VID 1 test point on the video output module (no. A22) front panel.

5. Adjust the VIDEO LEVEL control on the video output module for a signal amplitude of approximately 1 volt peak-to-peak at the VID IN test point.

6. Adjust potentiometer R17 (video/FM control module internal GAIN control) so that the white bar amplitude at the VID IN test point is equal to that at the VID 1 test point on the video output module. (Reduce the horizontal blanking width temporarily, utilizing the HOR BLKG WIDTH screwdriver control on the sync logic module, no. B21, in order to compare original black to white level without the effect of a new pedestal.)

7. Depress the VID OUT pushbutton on the CRO monitor switcher and observe the CRO monitor while performing steps 8 and 9 below.

8. Adjust the SYNC LEVEL control on the video output module to obtain a sync amplitude of 40 IRE units.

9. Adjust the PEDESTAL control on the video/FM control module for 7.5 IRE units pedestal and adjust the VIDEO LEVEL control on the video output module for 100 IRE units white bar.

10. Re-insert the video/FM control module into its receptacle and place the monochrome ATC delay/output module (no. B11) on the module extender.

11. Connect one probe of the external oscilloscope to the VID 1 test point on the demodulator output module front panel, and connect the other probe to the VID OUT 2 test point on the ATC delay/output module front panel.

12. Adjust potentiometer R3 (ATC delay/output module internal ATC LEVEL control) so that the white bar amplitude at the VID OUT 2 test point is equal to that at the VID 1 test point on the demodulator output module.

13. Re-insert the ATC delay/output module into its receptacle and place the color delay module (no. C12) on the module extender.

14. With one probe of the external oscilloscope remaining at the VID 1 test point on the demodulator output module, connect the other probe to the OUT test point on the color delay module front panel.

15. Adjust potentiometer R13 (color delay module internal COLOR ATC LEVEL control) so that the white bar amplitude at the OUT test point is equal to that at the VID 1 test point on the demodulator output module.

16. Rotate the mode selector switch on the ATC delay/output module to COLOR ATC or NON-PHASED COLOR position.

17. Re-insert the color delay module into its receptacle and place the chroma separator module (no. C13) on the module extender.

18. With one probe of the external oscilloscope remaining at the VID 1 test point on the demodulator output module, connect the other probe to the VID 1 test point on the video output module front panel.

19. Adjust potentiometer R3 (chroma separator module internal COLOR OUTPUT LEVEL control) so that the white bar amplitude at the VID 1 test point on the demodulator output module is equal to that at the VID 1 test point on the video output module.

20. Re-insert the chroma separator module into its receptacle.

TR-3 Machine Video Level

1. Set up the machine for simulated back-to-back operation as instructed in the *TR-3 Machine Setup* procedure at the beginning of this section, except that in step 2 rotate the mode selector switch on the monochrome ATC delay/output module (no. B11) to ATC OFF position.

2. Connect the external oscilloscope probe to the VID 3 test point on the demodulator output module (no. A18) front panel, and adjust the DEMOD LEVEL screwdriver control for a video amplitude of 1 volt peak-to-peak.

3. Place the video/FM control module (no. A21) on a module extender, and connect one probe of the external oscilloscope to the VID IN test point on the video control module front panel and connect the other probe of the external oscilloscope to the VID 1 test point on the video output module (no. A22) front panel.

4. Adjust the VIDEO LEVEL control on the video output module for a signal amplitude of approximately 1 volt peak-to-peak at the VID IN test point.

5. Adjust potentiometer R17 (video/FM control module internal GAIN control) so that the white bar amplitude at the VID IN test point is equal to that at the VID 1 test point on the video output module. (Reduce the horizontal blanking width temporarily, utilizing the HOR BLKG WIDTH screwdriver control on the sync logic module, no. B21, in order to compare original black to white level without the effect of a new pedestal.)

6. Observe the signal at the VID 1 test point on the video output module, utilizing the external oscilloscope, while performing steps 7 and 8 below.

7. Adjust the SYNC LEVEL control on the video output module to obtain a sync amplitude of 40 IRE units.

8. Adjust the PEDESTAL control on the video/FM control module for 7.5 IRE units pedestal and adjust the VIDEO LEVEL control on the video output module for 100 IRE units white bar.

9. Re-insert the video/FM control module into its receptacle and place the monochrome ATC delay/output module (no. B11) on the module extender.

10. Connect one probe of the external oscilloscope to the VID 1 test point on the demodulator output module front panel, and connect the other probe to the VID OUT 2 test point on the ATC delay/output module front panel.

11. Adjust potentiometer R3 (ATC delay/output module internal ATC LEVEL control) so that the white bar amplitude at the VID OUT 2 test point is equal to that at the VID 1 test point on the demodulator output module.

12. Re-insert the ATC delay/output module into its receptacle and place the color delay module (no. C12) on the module extender.

13. With one probe of the external oscilloscope remaining at the VID 1 test point on the demodulator output module, connect the other probe to the OUT test point on the color delay module front panel.

14. Adjust potentiometer R13 (color delay module internal COLOR ATC LEVEL control) so that the white bar amplitude at the OUT test point is equal to that at the VID 1 test point on the demodulator output module.

15. Rotate the mode selector switch on the ATC delay/output module to COLOR ATC or NON-PHASED COLOR position.

16. Re-insert the color delay module into its receptacle and place the chroma separator module (no. C13) on the module extender.

17. With one probe of the external oscilloscope remaining at the VID 1 test point on the demodulator output module, connect the other probe to the VID 1 test point on the video output module front panel.

18. Adjust potentiometer R3 (chroma separator module internal COLOR OUTPUT LEVEL control) so that the white bar amplitude at the VID 1 test point on the demodulator output module is equal to that at the VID 1 test point on the video output module.

19. Re-insert the chroma separator module into its receptacle.

Color Setup

1. Set up the machine for back-to-back (MOD-DEMOD) operation as instructed in the applicable *Machine Setup* procedure at the beginning of this section.

2. Place the color processor module (no. 231/C15) on the module extender and connect the external oscilloscope probe to the emitter of transistor Q23.

3. Adjust potentiometer R153 (color processor module internal CLAMP BAL control) so that the base-line during the vertical interval is aligned with the base-line during the remainder of the field.

4. Connect one of the external oscilloscope probes to the VID 1 test point on the video output module (no. 233/A22), and connect the other external oscilloscope probe to the OUT test point on the color delay module (no. 324/C12).

5. Adjust potentiometer R93 (color processor module internal CHROMA GAIN control) so that the chroma amplitude as observed at the OUT test point on the color delay module is equal to that observed at the VID 1 test point on the video output module.

6. Connect clip lead between pin 12 of the color processor module receptacle and chassis ground.

7. With the external oscilloscope probe remaining at the VID 1 test point on the video output module, make the following color processor module adjustments:

a. Adjust potentiometer R138 (internal DELAY control) for a 0.5 microsecond breezeway.

b. Adjust potentiometer R141 (internal WIDTH control) for 10 cycles of burst.

c. Adjust potentiometer R95 (BURST GAIN control on module front panel) for a burst amplitude of 0.3 volt (40 IRE units).

8. Remove clip lead from the color processor module receptacle, and re-insert the module into the machine.

Video Head Optimization (TR-22 and TR-4 Machines Only)

To obtain optimum results during recording, the record currents fed to each of the four video heads must be adjusted by setting the level controls on the record amplifier 1, 2, 3, and 4 modules (nos. 211 through 214/A3 through A6) so that the tape is just saturated when a normal input signal appears. The following procedure is a method of determining the optimum record currents for a particular headwheel panel.

Since the optimum currents change with video head wear, and the heads wear unequally, the procedure must be repeated whenever checks made during routine operation indicate that new optimum values are required. Two of these indications are (1) a poor signal-to-noise ratio, and (2) bands of unequal contrast.

Monochrome

1. Feed a monoscope signal, slide test pattern, or other similar test signal containing at least 30% peak whites, to the machine.

2. Thread a blank tape onto the machine and set the tape timer at zero.

3. In TR-22 machines place the microphone selector switch, located on the microphone module (no. 310) front panel, in AUD (audio) position.

In TR-4 machines place the microphone selector switch, located on the audio record module (no. B1) front panel, in MIC (microphone) position.

4. Operate the machine in SETUP mode.

5. In TR-22 machines, depress the AUDIO PB pushbutton (located directly below the VU meter)

and observe the VU meter while speaking into the microphone. Some movement of the VU meter indicator should be observed.

In TR-4 machines, rotate the VU meter selector switch on the playback control panel to program (PGM) REC position and observe the VU meter while speaking into the microphone. Some movement of the VU meter indicator should be observed.

6. Operate the machine in RECORD mode.

7. Set the LEVEL control on record amplifier 1 module (no. 211/A3) at 0 position, and announce the channel number and control position into the microphone. (E.g.: "This is channel no. 1 at zero.")

8. Rotate the LEVEL control toward no. 10 position, stopping at each digit to announce the position number in the microphone. When position no. 10 is reached repeat the procedure in reverse order, announcing the position numbers into the microphone at each digit until the control is returned to 0 position.

9. Set the LEVEL control at mid-range (position no. 5).

10. Repeat steps 7, 8, and 9 for channels 2, 3, and 4 (record amplifier modules 2, 3, and 4), and then re-wind the tape to the beginning of the test recording.

11. Set the EQUAL control on each of the four playback amplifier modules (nos. 215 through 218/A11 through A14) at the center of its range.

12. In TR-22 machines, rotate the FM EQ control on the FM equalizer module (no. 132) fully counterclockwise and then set the control one quarter turn (approximately 90 degrees) in the clockwise direction.

In TR-4 machines, rotate the FM EQUAL control on the video/FM control module (no. A21) fully counterclockwise and then set the control one quarter turn (approximately 90 degrees) in the clockwise direction.

13. Play back the tape in the tonewheel servo mode, depress the SW OUT pushbutton on the CRO monitor switcher, and adjust the C.T. PHASE control on the PLAY control panel to play back vertical sync on head no. 1.

14. While playing back the tape, observe the changing waveform pattern on the CRO monitor and listen to the audio playback to identify, in turn, the setting of each of the four record amplifier module LEVEL controls which produces maximum rf output.

15. Set each record amplifier module LEVEL control at its optimum position, as determined in step 14.

16. If more precise LEVEL control settings are required, the entire procedure may be repeated about each of the settings made in step 15, utilizing finer scale graduations. (E.g., if channel 1 is set at 4 in step 15, repeat step 8, utilizing positions 3.5, 4.0, and 4.5.)

17. After setting the LEVEL control on each of the record amplifier modules, record several minutes of the test signal fed to the machine in step 1. While recording, note the four record current readings corresponding to the optimum gain settings for future reference. (In TR-22 machines press the HD1, HD2, HD3, and HD4 pushbutton switches in succession and read the record currents on the d-c meter located above the tape transport panel. In TR-4 machines rotate the record current switch, located on the record control panel, through positions 1, 2, 3, and 4 in succession and read the record currents on the d-c meter located on the playback control panel.)

18. Re-wind the tape to the start of the recording made in step 17, and play the recording back.

19. While playing back the tape, adjust the LEVEL screwdriver controls on the playback amplifier 1, 2, 3, and 4 modules for equal amplitude (approximately 40 IRE units), as observed on the CRO monitor with the SW OUT pushbutton on the CRO monitor switcher depressed. *Do not set the levels too high.*

20. Set the EQUAL control on each of the four playback amplifier modules for proper equalization.

Color

Before color optimization may be accomplished, monochrome optimization must be completed as instructed in steps 1 through 20 above.

1. Apply a color bar test signal, having a split field with 100% white bar, to the video input of the machine and record 3 minutes of tape.

2. Re-wind the tape and play back the segment recorded in step 1.

3. Connect an external color monitor to the machine and depress the LINE OUT pushbutton on the color monitor switcher.

4. While observing the presentation on the color monitor, adjust the EQUAL control on the playback amplifier 1, 2, 3, and 4 modules (nos. 215 through 218/A11 through A14) to eliminate bands in the red bar. (The hue of the bar between channels should be identical.)

5. During the test playback, if a particular band in the yellow bar appears greenish, increase the record current for that particular video head by rotating the channel LEVEL control on the corresponding record amplifier module approximately one-half of a division in the clockwise direction. If a band in the yellow bar appears to be orange, decrease the record current for that particular head by rotating the LEVEL control approximately one-half of a division in the counterclockwise direction.

6. Make a second test recording and play the recording back.

7. Equalize each channel as instructed in step 4 and, if required, again adjust the record currents to correct orange and green banding in the yellow bar. Repeat this procedure until all bands in the yellow bar match.

8. Note the final record currents, as instructed in step 17 of the monochrome optimization procedure above, for future reference.

9. In TR-22 machines, depress the DEMOD OUT pushbutton on the CRO monitor switcher and, while observing the waveform on the CRO monitor, adjust the FM EQ control on the FM equalizer module (no. 132) front panel for normal chroma amplitude.

In TR-4 machines, depress the DEMOD OUT pushbutton switch on the CRO monitor switcher and, while observing the waveform on the CRO monitor, adjust the FM EQUAL control on the video/FM control module (no. A21) front panel for normal chroma amplitude.

International Standards Adjustments

The color ATC system has been adjusted at the factory for domestic (3.58 mc subcarrier) operation. Therefore, if the system is utilized in a machine operating on the proposed International (4.43 mc subcarrier) standards, the adjustment procedure presented below must be followed in addition to the preceding setup adjustments.

1. Set up the machine for back-to-back (MOD-DEMOD) operation as instructed in the applicable *Machine Setup* procedure at the beginning of the *Setup Adjustments* section, referring particularly to the *Note* in step 3.

2. Place the chroma separator module (no. 325/C13) on the module extender. Connect the external oscilloscope probe to the emitter of transistor Q35 and, with the oscilloscope sweep set for a horizontal rate presentation, tune inductor L1 for maximum burst.

3. Re-insert the chroma separator module into its receptacle and place the color sensor module (no. 323/C11) on the module extender. Connect the external oscilloscope probe to the emitter of transistor Q4 and, with the oscilloscope sweep set for a horizontal rate presentation, tune inductor L1 for maximum burst.

4. Re-insert the color sensor module into its receptacle and place the color error detector module (no. 326/C14) on the module extender. Connect the external oscilloscope probe to the emitter of transistor Q10 and, with the oscilloscope sweep set for a horizontal rate presentation, tune inductor L4 for maximum burst.

5. Reset potentiometer R94 (color error detector module internal ERROR CLAMP SET control) according to steps 7 and 8 of the *Color NLA/Error Detector Setup* procedure in the *Maintenance Adjustments* section below.

6. Re-insert the color error detector module into its receptacle and place the color processor module (no. 231/C15) on the module extender. Reset potentiometer R7 (color processor module internal SAW CENTERING control) according to steps 34 through 38 of the *Color NLA/Error Detector Setup* procedure in the *Maintenance Adjustments* section below.

MAINTENANCE ADJUSTMENTS

The maintenance adjustments presented in this section are provided as procedures to be followed when it is desired to set up the complete video system for optimum performance of the color ATC system.

Video Level

To correctly adjust the video level, follow the applicable *Video Level* adjustment procedure in the *Setup Adjustments* section.

Color Setup

1. Set up the machine for back-to-back (MOD-DEMOD) operation as instructed in the applicable *Machine Setup* procedure presented at the beginning of the *Setup Adjustments* section.

2. Place the chroma separator module (no. 325/C13) on a module extender.

3. Set the external oscilloscope sweep for a vertical rate presentation and connect the oscilloscope probe to the CHR OUT test point on the module front panel. Adjust potentiometer R10 (chroma separator module internal HI-PASS BALANCE control) so that the base-line during the vertical interval is aligned with the base-line during the remainder of the field.

4. Set the external oscilloscope sweep for a horizontal rate presentation, and connect one of the oscilloscope probes to pin 20 (ATC VID IN) of the chroma separator module plug and the other to the collector of transistor Q24. Adjust potentiometer R106 (chroma separator module internal GATE DELAY control) so that the delayed (positive-going) edge of the pulse at the collector of transistor Q24 trails the leading (negative-going) edge of ATC sync by 3.6 microseconds.

5. Connect the external oscilloscope probe to the emitter of transistor Q34, and adjust potentiometer R84 (chroma separator module internal BURST GATE WIDTH control) for a pulse width of 4.0 microseconds.

6. Connect the external oscilloscope probe to pin 21 (TAPE BURST OUT) of the chroma separator module plug and tune inductor L1 for maximum burst amplitude.

7. Re-insert the chroma separator module into its receptacle and place the color processor module (no. 231/C15) on the module extender.

8. Connect the external oscilloscope probe to the emitter of transistor Q23 and adjust potentiometer R153 (color processor module internal CLAMP BAL control) so that the base-line during the vertical interval is aligned with the base-line during the remainder of the field.

9. Connect one of the external oscilloscope probes to the VID 1 test point on the video output module (no. 233/A22) and connect the other probe to the OUT test point on the color delay module (no. 324/C12). Adjust potentiometer R93 (color processor module internal CHROMA GAIN control) so that the chroma amplitude observed at the OUT test point on the color delay module is equal to the chroma amplitude observed at the VID 1 test point on the video output module.

NOTE: It is very important that the various video gain controls be properly set up before setting the chroma gain.

10. Connect a clip lead from pin 12 of the color processor module plug to module ground.

11. While observing the video signal at the VID 1 test point on the video output module, make the following adjustments:

a. Adjust potentiometer R138 (color processor module internal DELAY control) for a 0.5 microsecond breezeway.

b. Adjust potentiometer R141 (color processor module internal WIDTH control) for 10 cycles of burst.

c. Adjust potentiometer R95 (BURST GAIN control on color processor module front panel) for a burst amplitude of 0.3 volt (40 IRE units).

12. Remove the clip lead connected in step 10 and re-insert the color processor module into its receptacle.

Burst Sensor Setup

1. Set up the machine for back-to-back (MOD-DEMOD) operation as instructed in the applicable *Machine Setup* procedure at the beginning of the *Setup Adjustments* section.

2. Place the color sensor module (no. 323/C11) on a module extender.

3. Set the external oscilloscope sweep for a horizontal rate presentation and connect the oscilloscope probe to the emitter of transistor Q2. Tune inductor L1 for maximum burst amplitude.

4. Set up the machine to play back a color test tape as instructed in the applicable *Machine Setup* procedure at the beginning of the *Setup Adjustments* section.

5. In TR-22 machines, connect the external oscilloscope probe to the TAPE BURST test point and adjust the FM EQ control on the FM equalizer module (no. 132) front panel for a burst amplitude of 1 volt peak-to-peak.

In TR-3/TR-4 machines, connect the external oscilloscope probe to the TAPE BURST test point and adjust the FM EQUAL control on the video/FM control module (no. A21) front panel for a burst amplitude of 1 volt peak-to-peak.

6. Set the external oscilloscope sweep for a vertical rate presentation and, with the oscilloscope input on DC, connect the oscilloscope probe to the collector of transistor Q7. Adjust potentiometer R9 (color sensor module internal BURST SENSOR THRESHOLD control) so that transistor Q7 just begins to conduct (i.e., the collector potential rises from −26 volts dc to ground). Then adjust the potentiometer one full turn in the clockwise direction.

Color Non-Linear Amplifier (NLA) Error Detector Setup

1. Set up the machine for back-to-back (MOD-DEMOD) operation as instructed in the applicable *Machine Setup* procedure at the beginning of the *Setup Adjustments* section.

2. Place the color error detector module (no. 326/C14) on the module extender.

3. With the external oscilloscope sweep set for a horizontal rate presentation, connect the oscilloscope probe to the emitter of transistor Q10 and tune inductor L4 for maximum burst amplitude. (While tuning inductor L4 place a flat metal plate, wrapped with tape to protect the components, over the module to simulate inter-module shielding.)

NOTE: For a precise adjustment of inductor L4 refer to the adjustment procedure following the color error detector module circuit description.

4. With the external oscilloscope sweep set for a subcarrier rate presentation, connect both oscilloscope probes to terminal 5 of transformer T1, set the oscilloscope for a DC input on each probe, and match the probes for vertical gain and vertical position (approximately 0.5 volt/cm).

5. Expand the external oscilloscope sweep rate to 0.1 microsecond/cm, and adjust the SYSTEM PHASE control on the color phase module (no. 232/C16) front panel so that the pip (appearing during the burst interval) falls at the center of the slope.

6. Remove one of the external oscilloscope probes from terminal 5 of transformer T1, connect it to the junction of resistors R133 and R134, and adjust potentiometer R132 (color error detector module internal ERROR BAL control) so that the d-c signal at the junction of R133 and R134 falls at the same level as the pip on the slope.

7. Connect the external oscilloscope probe to the emitter of transistor Q32 and set the SYSTEM PHASE control, on the color phase module front panel, at the point where the error signal indicates sampling over the extremes of the sampling range. With the external oscilloscope sweep set for a vertical rate presentation, adjust the oscilloscope vertical gain and vertical centering controls so that the sampling extremes are symmetrical about the horizontal center-line of the oscilloscope graticule (±2 divisions).

8. Connect the external oscilloscope probe to the base of transistor Q31 and adjust potentiometer R94 (color error detector module internal ERROR CLAMP SET control) so that the d-c signal falls at the horizontal center-line of the oscilloscope graticule.

9. Connect an external oscilloscope probe to the emitter of transistor Q32 and adjust the oscilloscope sweep for a horizontal rate presentation. While observing the error signal on the oscilloscope, adjust potentiometer R171 (LEAKAGE CANCEL ADJ) to obtain a straight, horizontal line between horizontal samples.

10. Re-insert the color error detector module into its receptacle and place the color processor module (no. 231/C15) on the module extender.

11. Connect the vacuum-tube voltmeter between pin 13 of plug P1 (delay line centering potential) and module ground, and adjust potentiometer R156 (color processor module internal DELAY LINE REFERENCE ADJ control) for a delay line reference potential of −9.7 volts with respect to ground.

CAUTION: Make certain the VTVM case is insulated from ground when making these adjustments.

12. Connect the vacuum-tube voltmeter between pin 13 of plug P1 and the base of transistor Q16, and adjust potentiometer R64 (color processor module internal DELAY LINE CENTER control) so that the potential at the base of Q16 is +2.9 volts with respect to the delay line reference potential at pin 13.

13. Connect a clip lead between the base of transistor Q2 and ground.

14. Connect the vacuum-tube voltmeter between pins 13 and 21 (NEB output) of plug P1, and adjust potentiometer R36 (color processor module internal NEB DC SET control) for a NEB potential of −0.5 volt with respect to the delay line reference potential.

15. Connect the vacuum-tube voltmeter between pins 13 and 20 (PEB output) of plug P1, and adjust potentiometer R40 (color processor module internal PEB DC SET control) for a PEB potential of +0.5 volt with respect to the delay line reference potential.

16. Remove the clip lead connected in step 13 above.

17. Matrix PEB and NEB potentials at the PEB and NEB test points on the color delay module (no. 324/C12) front panel, utilizing two 20K-ohm, 1%, resistors.

18. A-c couple the external oscilloscope to the matrixed PEB and NEB potentials, and set up the oscilloscope for a 1 millisecond/cm sweep rate ("A" trace) and a .02 volt/cm vertical gain.

19. Set up the machine to play back a color test tape as instructed in the applicable *Machine Setup* procedure at the beginning of the *Setup Adjustments* section.

20. In TR-22 machines, place the vacuum guide in MANUAL mode and decrease the guide pressure utilizing the GUIDE POSITION control on the RECORD control panel.

In TR-3/TR-4 machines, turn the rubber roller on the right-hand side of the headwheel cover in a clockwise direction to decrease the vacuum guide pressure.

21. Reduce the monochrome ATC error gain slightly, utilizing the ERR GAIN screwdriver control on the ATC reference module (no. 226/B14) front panel, so that some guide error appears in the color ATC signal. *Do not exceed the color ATC error signal range.* (In TR-22 machines the color error signal may be observed on the CRO monitor when the CATC ERR pushbutton on the CRO monitor switcher is depressed. In TR-3/TR-4 machines, the color error signal may be observed by connecting an external oscilloscope probe to the ERR OUT test point on the color error detector module.)

22. Re-adjust potentiometer R40 (PEB DC SET) to minimize 16-line steps.

23. Rotate potentiometers R48 (PEB AC SET) and R44 (NEB AC SET) fully clockwise, and then rotate potentiometer R48 counterclockwise to minimize 16-line spikes.

24. Increase the vacuum guide pressure so that a guide error of opposite polarity appears in the color ATC signal.

25. Rotate potentiometer R44 counterclockwise to minimize 16-line spikes.

26. Set up the machine for back-to-back (MOD-DEMOD) operation as in step 1 above.

27. Connect a clip lead between the base of transistor Q2 and module ground.

28. Connect the vacuum-tube voltmeter negative lead to pin 13 of plug P1 (delay line reference potential), measure the PEB potential at pin 20 and NEB potential at pin 21, and re-adjust potentiometer R156 (DELAY LINE REFERENCE ADJ) to split the error difference so that the PEB and NEB potentials are equal and opposite with respect to the delay line reference potential.

29. With the negative lead of the vacuum-tube voltmeter remaining on pin 13 of plug P1, re-adjust potentiometer R36 (NEB DC SET) to obtain a NEB potential at pin 21 (NEB output) equal to −0.5 volt with respect to the delay line reference potential.

30. Remove the clip lead connected in step 27.

31. Repeat steps 19 through 22 and, if necessary, steps 23 through 25 above.

32. If potentiometer R40 (PEB DC SET) required re-adjustment in step 31, repeat steps 26 through 32.

33. Reset monochrome ATC error gain screwdriver control (on the monochrome ATC reference module front panel) and vacuum guide control to their normal positions.

34. Set up the machine to play back a color test tape as in step 19 above.

35. Connect the external oscilloscope probe to pin 17 of plug P1 (error input), utilizing a 10:1 attenuation probe, and connect the vacuum-tube voltmeter between pins 13 and 20 of plug P1. Adjust potentiometer R64 (color processor module internal DELAY LINE CENTER control) to obtain a PEB potential of +2.9 volts with respect to the delay line reference potential.

36. Adjust the external oscilloscope vertical gain and centering so that the full range of the color ATC error signal (observable during "lock-up") covers 4 cm at the center of the oscilloscope graticule.

37. Adjust potentiometer R7 (color processor module internal SAW CENTERING control) so that the average error signal falls at the center of the range established in step 36.

38. Repeat steps 35 and 37.

39. Set up the machine for back-to-back (MOD-DEMOD) operation as in step 1 above.

40. Place the color error detector module on a second module extender.

> NOTE: Since the color processor and color error detector modules are adjacent in TR-3/TR-4 machines, it will not be possible to place both modules on extenders simultaneously. Therefore, in these machines it will be necessary to make trial adjustments in step 41 below until the correct setting of potentiometer R94 is attained.

41. Connect the vacuum-tube voltmeter between the PEB test point on the color delay module and pin 13 of plug P1 (delay line reference) on the color processor module, and adjust potentiometer R94 (color error detector module internal ERROR CLAMP SET control) so that the error signal is clamped at a PEB potential of +2.9 volts with respect to the delay line reference potential.

Color Sensor Delay

1. Place the color sensor module (no. 323/C11) on the module extender.

2. Set up the machine for back-to-back (MOD-DEMOD) operation as instructed in the applicable *Machine Setup* procedure at the beginning of the *Setup Adjustments* section.

3. Connect the external oscilloscope probe to the collector of transistor Q15 and adjust potentiometer R44 (color sensor module internal DELAY ADJ control) for a pulse width of 7.5 microseconds.

4. Re-insert the color sensor module into its receptacle.

Delay Line Termination Adjustments

The color fixed delay line mounted at the rear of TR-22 machines, the color fixed delay module in TR-3/TR-4 machines, and the electronically variable delay lines contained in the color phase module (no. 232/C16) and color delay module (no. 324/C12), all have terminations which are adjustable by means of potentiometers. These potentiometers have been adjusted for optimum color ATC system performance at the factory, utilizing equipment not generally available in most television studios, and it is extremely unlikely that any re-adjustment will be required. Therefore, unless trouble in the color ATC system is traced directly to the delay line terminations, *do not change the setting of any termination potentiometer.*

Component failure within a delay line unit cannot be compensated for by adjusting the associated termination potentiometer. However, since the possibility of inadvertently misadjusting a termination potentiometer exists, an emergency re-adjustment procedure is presented below.

> NOTE: Before making any adjustments it is advisable to mark the present potentiometer setting by some convenient means (e.g., a scribe mark on the shaft).

Test equipment required for termination potentiometer re-adjustment includes the following:

75-ohm Attenuator

Video Sweep Generator *(Marconi Model 1099* or equivalent)

Dual-Trace Oscilloscope *(Tektronix Type 535A,* or *Type 545A* with CA plug-in, or equivalent)

Vacuum-Tube Voltmeter *(RCA Type WV-98A Voltohmyst,* or equivalent)

A. Fixed Delay Line Terminations

TR-22 Machines:

1. Disconnect the coax cables from the input and output jacks (J1 and J2) of the fixed delay line FDL2 which is mounted at the rear of the machine.

2. Connect a length of RG59U cable between the delay line output (jack J2) and the oscilloscope input, utilizing a T connector at the oscilloscope. Terminate the line at the T connector with 75 ohms.

3. Connect the sweep generator to the delay line input (jack J1). Adjust the generator for a sweep range of 1 to 11 mc and an output signal amplitude of 1 volt peak-to-peak at 5 mc.

4. Remove the delay line cover.

5. While observing the oscilloscope, tune inductor L59 to obtain the flattest overall frequency response, referenced to the sweep generator output, between 1 and 6 mc. The response should be flat $\pm 5\%$ to 5.0 mc, $\pm 10\%$ to 7.0 mc, and cut off at approximately 9.5 mc.

6. Alternately adjust termination potentiometers R2 and R4 to minimize ripple at 1 and 8 mc. (The delay line output level should not be less than 0.38 volt peak-to-peak when the potentiometers have been adjusted.)

7. Disconnect the sweep generator from the delay line input (jack J1) and feed a video signal to the delay line.

8. With the oscilloscope "B" input connected to the delay line output jack as in step 2 above, connect the oscilloscope "A" input to the delay line input jack.

9. Place the oscilloscope selector switch in ALTERNATE position, and observe the delay generated by the delay line. The delay, as observed on the oscilloscope, should be approximately 2.7 microseconds.

10. Remove the oscilloscope and video input cables, replace the delay line cover, and re-connect the coax cables to the fixed delay line input and output jacks (J1 and J2).

TR-3/TR-4 Machines:

1. Remove the color fixed delay line module (no. 3A3) from the machine.

2. Connect one end of a length of RG59U cable to the oscilloscope input, utilizing a T connector at the oscilloscope. Terminate the line at the T connector with 75 ohms. Connect the center conductor of the other end of the cable to the fixed delay line module output at pin 18, and connect the cable shielding to pin 20.

NOTE: Optimum results may be obtained by soldering the center conductor and shielding to the respective delay line module pins.

3. Connect the center conductor of a shielded lead from the sweep generator to the fixed delay line module input at pin 2, and connect the cable shielding to pin 4. (See *Note* below step 2 above.) Adjust the generator for a sweep range of 1 to 11 mc and an output signal amplitude of 1 volt peak-to-peak at 5 mc.

4. While observing the oscilloscope, tune inductor L59 to obtain the flattest overall frequency response, referenced to the sweep generator output, between 1 and 6 mc. The response should be flat $\pm 5\%$ to 5.0 mc, $\pm 10\%$ to 7.0 mc, and cut off at approximately 9.5 mc.

5. Adjust termination potentiometer R4 to minimize ripple at 1 and 8 mc. (The delay line output level should not be less than 0.38 volt peak-to-peak when the potentiometer has been adjusted.)

6. Disconnect the sweep generator and feed a video signal to the fixed delay line input. (See *Note* below step 2 above.)

7. With the oscilloscope "B" input connected to the fixed delay line output as in step 2 above, connect the oscilloscope "A" input to the fixed delay line input.

8. Place the oscilloscope selector switch in ALTERNATE position, and observe the delay generated by the delay line. The delay, as observed on the oscilloscope, should be approximately 2.7 microseconds.

9. Remove the oscilloscope and video input cables, and re-insert the fixed delay line module into its receptacle.

B. Color Delay Module Delay Line Terminations

1. In TR-22 machines, disconnect the coax cable from jack J2 of the fixed delay line FDL2 at the rear of the machine, and connect the cable to the output jack of the 75-ohm attenuator.

In TR-3/TR-4 machines, remove the color fixed delay line module (no. 3A3) from the machine and connect a shielded lead between pins 18 and 20 of the fixed delay line module receptacle (at the rear of the machine) and the 75-ohm attenuator output jack. (Make certain the center conductor of the shielded lead is connected to pin 18 and the shielding to pin 20.)

2. Connect the sweep generator output to the 75-ohm attenuator input jack, and set the attenuator at -8 db.

3. Connect the oscilloscope trigger input to the time base terminal of the sweep generator.

4. Place the color delay module (no. 324/C12) on the module extender.

5. Set up the machine for back-to-back (MOD-DEMOD) operation as instructed in the applicable *Machine Setup* procedure at the beginning of the *Setup Adjustments* section.

6. Connect one of the oscilloscope probes to the video input of the color delay module (at the junction of resistor R14 and the coax cable from pin 17 of plug P1).

7. Connect the other oscilloscope probe to the sweep generator marker output.

8. Set the sweep generator for a sweep width out to 15 mc, and adjust the generator output for an amplitude of 0.4 volt peak-to-peak as observed on the oscilloscope.

9. Connect the common lead of the vacuum-tube voltmeter to the delay line center (at the junction of 10K-ohm resistor R22 and disc capacitor C11). ***Make certain the voltmeter case is insulated from ground.***

10. Measure the NEB and PEB voltages at the NEB and PEB test points to ascertain that they are -2.9 and $+2.9$ volts dc respectively. (If they are not, refer to steps 10 through 16 of the *Color NLA/Error Detector* adjustment procedure.) Remove the voltmeter after the measurements have been made.

11. Remove the oscilloscope probe from the video input (junction of resistor R14 and the coax cable), and connect it to the OUT test point.

12. Adjust potentiometer R13 (color delay module internal COLOR ATC LEVEL control) to obtain a sweep signal amplitude of 1 volt peak-to-peak at the OUT test point, as observed on the oscilloscope.

13. While observing the oscilloscope, adjust the 500-ohm terminating potentiometers R2 and R18 to minimize ripple in the response out to 8.0 mc.

14. Adjust variable capacitor C3 to obtain a flat response at the OUT test point. The response should be flat to 8.0 mc (i.e., down by no more than 5% at 8.0 mc), and the signal should be completely cut off at approximately 12.5 mc.

NOTE: If the response exhibits excessive peaks and dips, the delay line is faulty. Due to the complexity of repair techniques, the *RCA Service Company* should be consulted if it is determined that the delay line is faulty.

15. Disconnect the sweep generator and attenuator, and re-connect the coax cable to jack J2 of fixed delay line FDL2 in TR-22 machines or, in TR-3/TR-4 machines, re-insert the fixed delay line module (no. 3A3) into its receptacle.

16. Rotate the selector switch on the ATC delay/output module (no. 223/B11) to ATC OFF position.

17. Adjust the oscilloscope for equal gain in both input channels and, with one oscilloscope probe remaining on the OUT test point, connect the other oscilloscope probe to the VID 1 test point on the demodulator output module (no. 303/A18).

18. Adjust potentiometer R13 (color delay module internal COLOR ATC LEVEL control) so that the amplitude of the signal observed at the OUT test point is equal to the amplitude of the signal appearing at the VID 1 test point.

19. Re-insert the color delay module into its receptacle.

C. Color Phase Module Delay Line Terminations

1. Disconnect the coax cables from jacks J5 and J6 (SC IN) on the connector board at the bottom of the machine, and connect a 75-ohm termination plug to either J5 or J6. (In TR-3/TR-4 machines, disconnect the coax cables from both SC IN jacks mounted on the connector board at the rear of the machine and connect a 75-ohm termination plug to either jack.)

2. Connect the sweep generator output to the SC IN jack which has not been terminated.

3. Connect the oscilloscope trigger input to the time base terminal of the sweep generator.

4. Place the color phase module (no. 232/C16) on the module extender.

5. Connect one of the oscilloscope probes to the local subcarrier input to the color phase module (at the junction of capacitor C17 and the coax cable from pin 17 of plug P1), and connect the other oscilloscope probe to the sweep generator marker output.

6. Set the sweep generator for a sweep width out to 15 mc, and adjust the generator output for an amplitude of 2.0 volts peak-to-peak as observed on the oscilloscope.

7. Remove the oscilloscope probe from the subcarrier input and connect it to the SSC OUT test point.

8. Adjust the SYSTEM PHASE control, on the module front panel, to the center of its range.

9. While observing the oscilloscope, adjust the delay line termination potentiometer R40 (DL2 TERM) to minimize ripple in the response.

10. Check the response with the SYSTEM PHASE control adjusted to positions near the extremes of its range. The final adjustment of termination potentiometer R40 should be that which results in the lowest ripple over the entire range of the SYSTEM PHASE control. Ripple should not exceed 5% of the signal amplitude to 7.0 mc, and the frequency response should not be down more than 10% at 7.0 mc in comparison with that at 1.0 mc.

NOTE: If the response exhibits excessive ripple, the delay line is faulty. Due to the complexity of repair techniques, the *RCA Service Company* should be consulted if it is determined that the delay line is faulty.

11. Remove the oscilloscope probe from the SSC OUT test point and connect it to the BSC OUT test point. Set the SYSTEM PHASE control at the center of its range. Repeat steps 8, 9, and 10, utilizing the BURST PHASE control and delay line termination potentiometer R28 (DL1 TERM).

12. Disconnect the sweep generator and attenuator plug and re-connect the coax cables to the SC IN jacks.

13. Re-insert the color phase module into its receptacle.

MODULE CIRCUIT ANALYSES

A detailed circuit analysis of each of the six individual modules which are contained in the color ATC system is presented in this section. Each module circuit analysis is followed by detailed adjustment procedures for that particular module. Partial schematic diagrams are intended to show only the area under discussion. For a complete schematic diagram of each individual module refer to the rear of this instruction book. Functional block diagrams of the color ATC system and control functional diagrams which will prove useful in following the individual module circuit analyses, are also located at the rear of this instruction book.

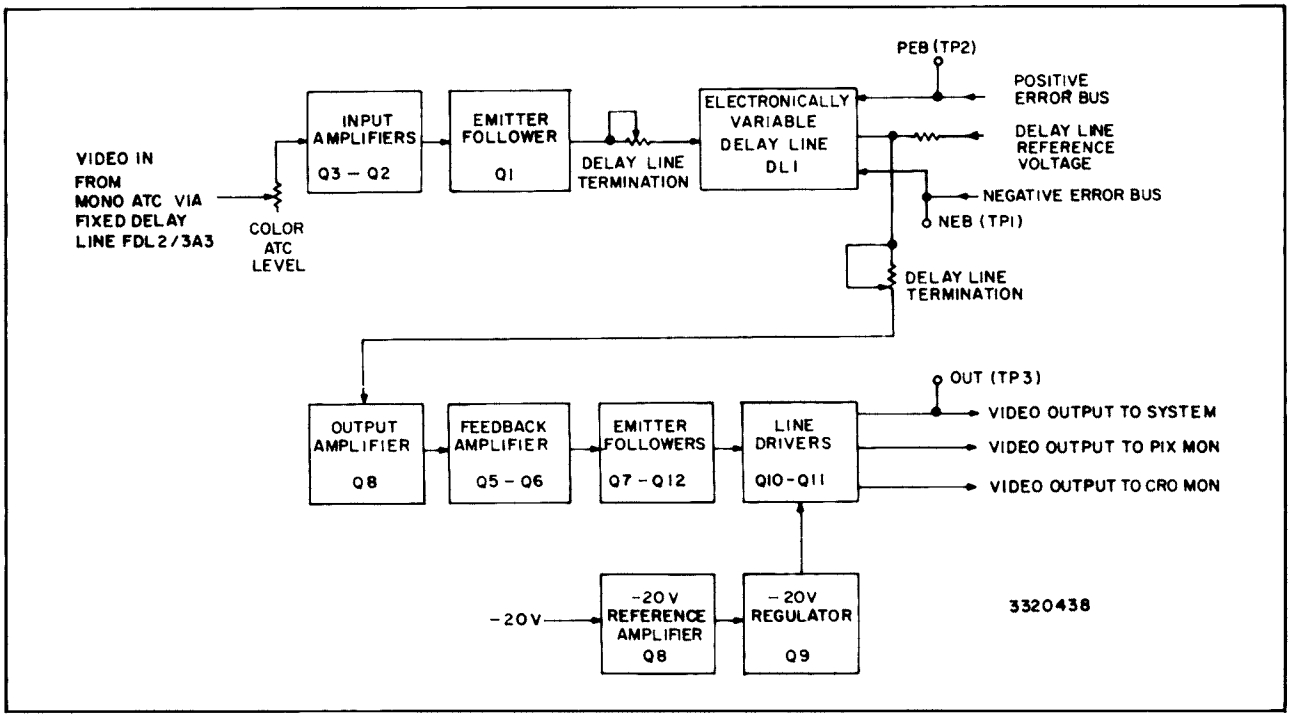


Figure 13—Color Delay Module Block Diagram

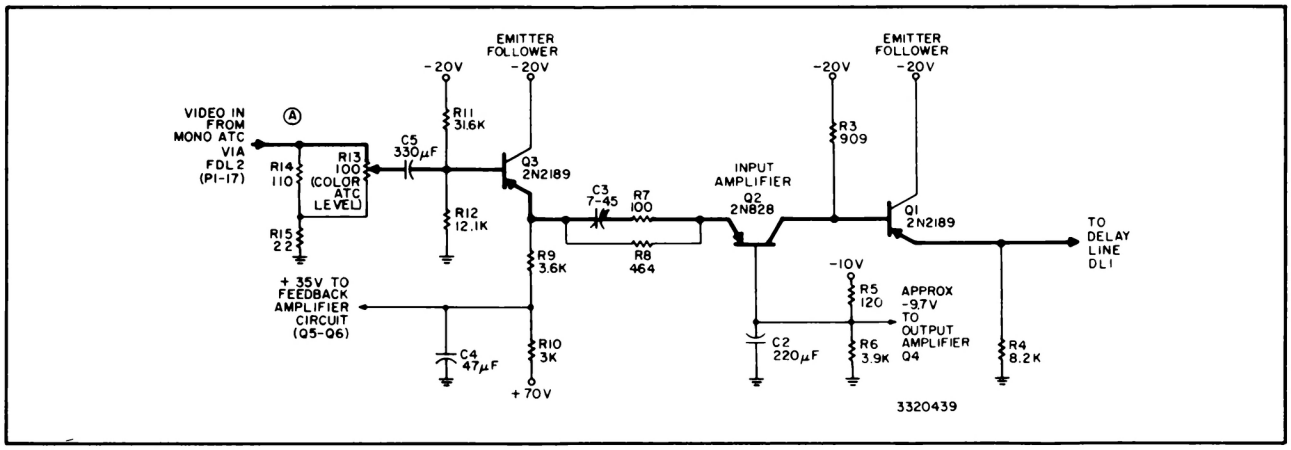
COLOR DELAY MODULE, 324/C12

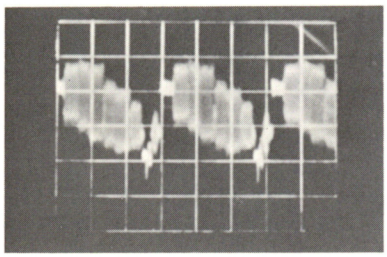
Circuit Description

General

The tape video signal is fed to the color delay module (no. 324/C12) from the monochrome ATC system after being delayed by the fixed delay line FDL2/3A3. (See block diagram, figure 13.) In the color delay module, further correction of timing errors in the video signal is accomplished by passing the signal through an electronically variable delay line whose delay is controlled by the error signal developed from a phase comparison of tape burst and reference subcarrier signals in the color error detector module (no. 326/C14). Due to the sampling of the reference subcarrier by tape burst, transients appear on the error busses. Since the tape burst information, from which the sample pulses are derived, is taken off ahead of the fixed delay line FDL2/3A3, the transients applied to the variable delay line will be advanced 2.5 microseconds (the delay of FDL2/3A3) with respect to the composite video signal. Therefore the transients will occur during the horizontal sync pulse interval and thus will not affect the burst or video information in the composite signal. The output of the variable delay line is then the composite video signal which has been stabilized in time with respect to the local subcarrier signal.

A driver circuit drives the corrected video signal to the chroma separator module (no. 325/C13) in the color ATC system, and to the CRO monitor and the picture monitor. The color delay module also includes a −20 volt regulator circuit which effectively de-couples the −20 volt bus and provides the current required by the output driver circuit.





A. Video Input (P1-17), lv/cm. (20 μsec/cm)

Playback in COLOR ATC mode.

Figure 14—Input Video Amplifier

Input Video Amplifier

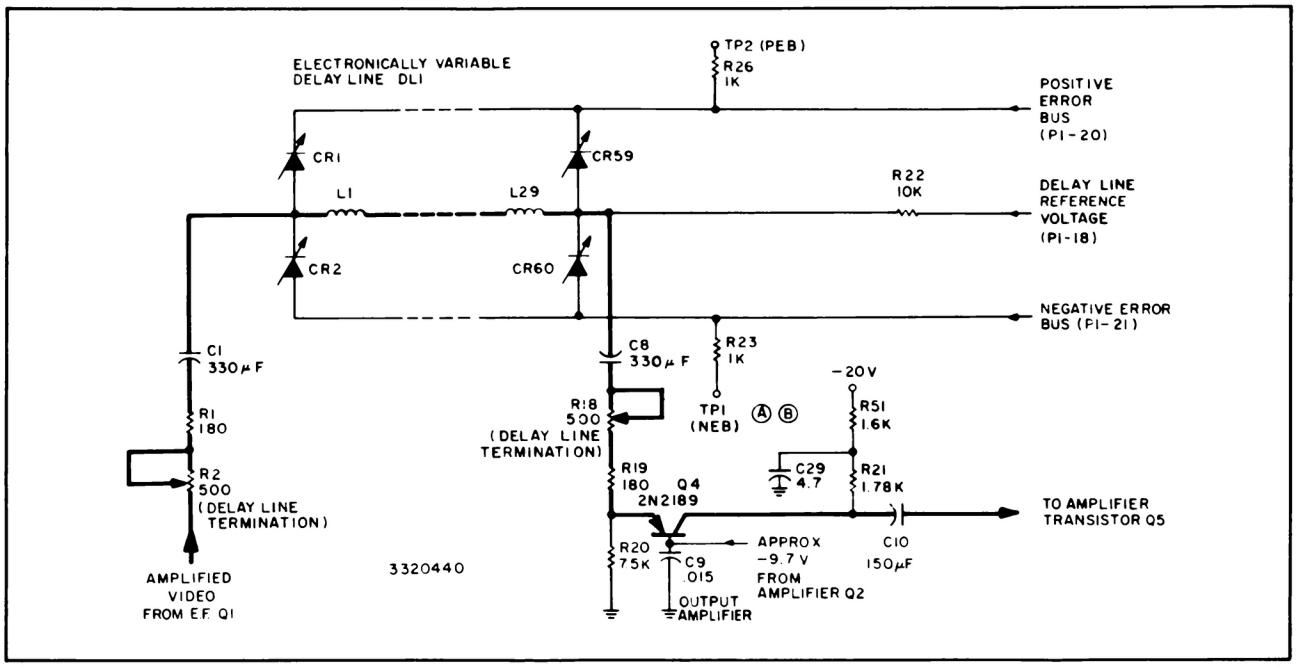
The incoming tape video signal at pin 17 of plug P1 (figure 14A) is applied across resistor R15 in series with resistor R14 and potentiometer R13 in parallel. Potentiometer R13 is utilized in setting the level of the video output from the color delay module at 1 volt peak-to-peak. (See *Adjustments.*) From potentiometer R13, the video signal is capacitance coupled to the base of emitter follower transistor Q3. Transistor Q3, biased into conduction by the voltage divider network (R11, R12) in its base circuit, isolates the succeeding amplification circuitry from the relatively low impedance fixed delay line FDL2/3A3. The video signal at the emitter of transistor Q3 is then fed through the high frequency compensation network, consisting of resistors R7, R8 and variable capacitor C3, to the emitter of amplifier transistor Q2. Capacitor C3 may be varied over a range of 7 to 45 micromicrofarads, and is utilized in peaking the high frequency components of the video signal so that the overall frequency response of the color delay module circuitry is flat.

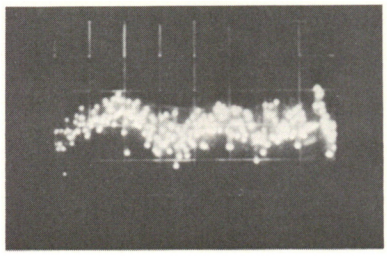
During normal operation a current of approximately 12 milliamperes flows through resistor R10 in the emitter circuit of transistor Q3, and this results in a potential of approximately +35 volts at the junction of resistors R9 and R10. Capacitor C4, functioning as a low frequency bypass capacitor, minimizes fluctuations which may otherwise appear in the +35 volt potential. The potential thus obtained is utilized in the feedback amplifier circuit which is discussed below.

Transistor Q2, biased into conduction by a potential of approximately −9.7 volts dc applied to its base from the voltage divider network consisting of resistors R5 and R6, is operated as an a-c common base amplifier. The amplified video signal appearing at the collector of transistor Q2 is fed directly to the base of emitter follower transistor Q1. Transistor Q1 isolates the amplification circuit from the low impedance electronically variable delay line which follows, and the video signal at the emitter of Q1 is then capacitance coupled to the delay line.

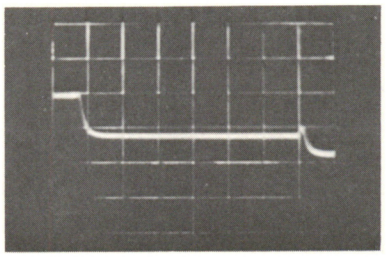
Delay Line and Output Amplifier

Delay line DL1 consists of inductors and silicon diodes whose individual capacitances are inversely proportional to the magnitude of the potential impressed across them. Thus as the potential increases,





A. TP1 (NEB).
Vertical rate sweep.



B. TP1 (NEB).
Horizontal rate sweep.

Playback in COLOR ATC mode.

Figure 15—Delay Line and Output Amplifier Circuits

the capacitance of the diodes, and therefore the delay introduced, decreases (and vice versa). A single-ended video signal is fed to the delay line; however, control of the line is push-pull (positive and negative d-c potentials with respect to that at the mid-point of the delay line) so that transients, which are coupled from the control busses to the video path by the capacitance of the delay line diodes each time the control voltage changes, will be cancelled out. The delay line diodes represent a capacitive load and for proper operation of the delay line a fairly rapid response must be achieved, during which time the positive and negative error busses (PEB and NEB) must remain accurately balanced to achieve the desired transient cancellations.

As the diode capacitance is modulated by the changing error control voltage, both the delay and the characteristic impedance of the delay line will change. Thus as modulation away from the center of the delay range takes place, an increasing mis-termination results. The delay line is terminated at both its input and output by termination networks which include potentiometers R2 and R18. The potentiometers provide a means of varying the termination network impedance so that impedance matching may be obtained which will allow the delay line to pass a wide band of frequencies, without excessive high frequency roll-off, over the entire delay range. To obtain optimum impedance matching, termination potentiometers R2 and R18 have been precisely adjusted at the factory and, since their settings are critical, *no attempt should be made to re-adjust them.* (In the event that one or both termination potentiometers become inadvertently mis-adjusted, an emergency adjustment procedure is provided below under *Adjustments.*)

The delay line control voltage consists of potentials which are positive and negative with respect to a fixed reference voltage of −10 volts. The positive and negative potentials are generated in the color processor module (no. 231/C15) from a phase comparison of burst separated from the undelayed tape video signal and the reference subcarrier signal. The positive error potential is applied to delay line DL1 from the positive error bus via pin 20 of plug P1, and may be observed at test point TP2 (PEB). The negative error potential is applied to the delay line from the negative error bus via pin 21 of plug P1, and may be observed at test point TP1 (NEB). (Refer to figure 15A for a vertical rate presentation of the negative error signal observed at test point TP1, and to figure 15B for a horizontal rate presentation of the negative error signal.) The reference voltage (−10 volts dc), also obtained from the color processor module, is fed to the mid-point of the delay line via pin 18 of plug P1.

For proper operation of the color ATC system, it is essential that the delay of the delay line vary linearly with respect to the error voltage from the phase detector. The capacitance vs. voltage characteristic of the silicon diodes in the delay line is highly non-linear and, in addition, the delay varies as the square root of the capacitance. To correct for this non-linearity, a non-linear amplifier (located in the color processor module) is placed in the control voltage path.

The delay line is designed to operate with the application of voltages ranging from 1 to 8 volts across each set of diodes. However, due to the non-linear characteristics of the delay line, the mid-point of the delay range is attained when a voltage of 2.9 volts is applied to the diodes. Therefore the diodes are clamped at 2.9 volts whenever the machine is in the STOP mode or in non-color operation due to lack of burst, lack of pixlock, etc., and the delay line terminations are adjusted for this voltage. During machine operation in the color ATC mode, the system adjustments are such that when pulses generated from tape burst sample at the center of the reference sawtooth waveform the voltage across each set of diodes is 2.9 volts. The PEB potential is then −7.1 volts and the NEB potential is −12.9 volts. This represents a potential difference of 2.9 volts between both the PEB and NEB and delay line mid-point, and corresponds to a delay of approximately 1.1 microseconds. If a phase shift occurs between the undelayed tape burst and reference subcarrier, an error signal is developed in the color processor module which causes the PEB and NEB potentials to change by equal amounts and a corresponding delay results. When the PEB potential reaches −2 volts (+8 volts with respect to the reference voltage) the NEB potential is −18 volts and the potential across delay line DL1 is at its maximum value. This results in minimum delay line diode capacitance and therefore minimum delay. Conversely, when the PEB potential reaches −9 volts (+1 volt with respect to the reference voltage) the NEB potential is −11 volts and the potential across DL1 is at its minimum value. This in turn results in maximum diode capacitance and therefore maximum delay. As the potential across DL1 varies from its maximum to its minimum value, the delay generated varies between the approximate limits of 0.95 and 1.25 microseconds. The nominal delay range of delay line DL1 is thus approximately 0.3 microsecond, which corresponds to a subcarrier phase shift in excess of 360 degrees.

The delayed video signal is capacitance coupled to a-c common base amplifier transistor Q4. Transistor Q4 acts as an impedance transformer, and the amplified video signal appearing at the collector of Q4 is then coupled to the base of amplifier transistor Q5.

Feedback Amplifier

Figure 16 shows the feedback amplifier circuit. The purpose of this circuit is to stabilize gain over the wide range of frequencies contained in the video signal and, more specifically, to maintain the subcarrier frequency component of the video signal (3.58 mc in machines operating on 525-line standards; 4.43 mc on machines operating on 625-line standards) at a constant level regardless of the delay presented by delay line DL1. Gain stabilization is achieved by means of a negative feedback loop which is frequency controlled through the use of silicon diodes operating in exactly the same manner as are those in delay line DL1. Negative feedback results in an overall reduction in gain; however the higher frequency components of the video signal are bypassed to ground by the frequency controlled bypass network and therefore do not contribute to the negative feedback. Thus the higher frequency components of the signal are in effect boosted to compensate for roll-off which occurs as the video signal passes through delay line DL1.

The video signal from amplifier transistor Q4 is coupled to the base of transistor Q5. Transistor Q5 is biased into conduction by the potential applied to its base from the divider network consisting of resistors R26, R33, and R34 connected between +35 volts dc from the emitter circuit of transistor Q3 and the emitter potential of transistor Q6. The video

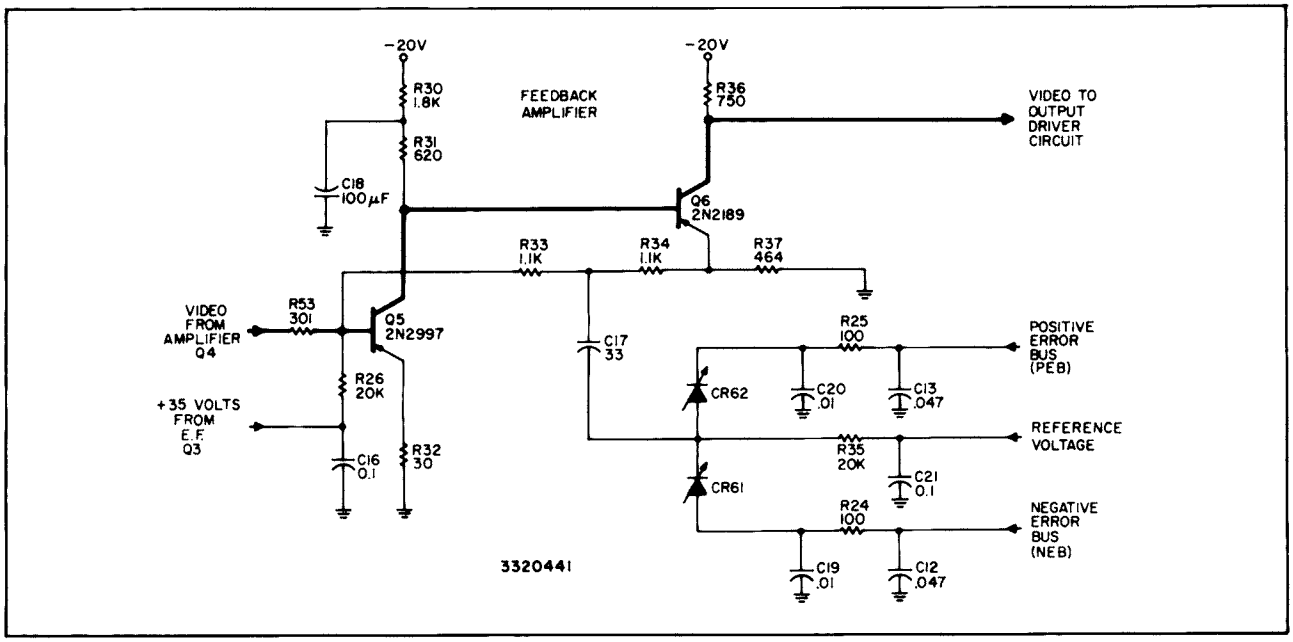


Figure 16—Feedback Amplifier

signal at the collector of transistor Q5 is then fed directly to the base of transistor Q6. Transistor Q6 amplifies the video signal, and the amplified signal appearing at its collector is in turn fed directly to the base of emitter follower transistor Q7 in the output driver circuit.

The video signal applied to the base of transistor Q6 also appears at the emitter of Q6. Negative feedback is accomplished by feeding the video signal at the emitter of Q6 back to the base of transistor Q5, where it arrives 180 degrees out of phase with the signal applied to Q5 from amplifier transistor Q6. The negative feedback path includes resistors R33 and R34, and a high frequency bypass network. Essentially, the high frequency bypass network consists of capacitor C17 in series with the paralleled silicon diodes CR61 and CR62. As in delay line DL1, the capacitance of each silicon diode is an inverse function of the potential impressed across it. This potential is obtained from the positive and negative error busses (PEB and NEB); thus the capacitance of diodes CR61 and CR62 varies in accordance with the error developed from the phase comparison of undelayed tape burst and the local subcarrier signal.

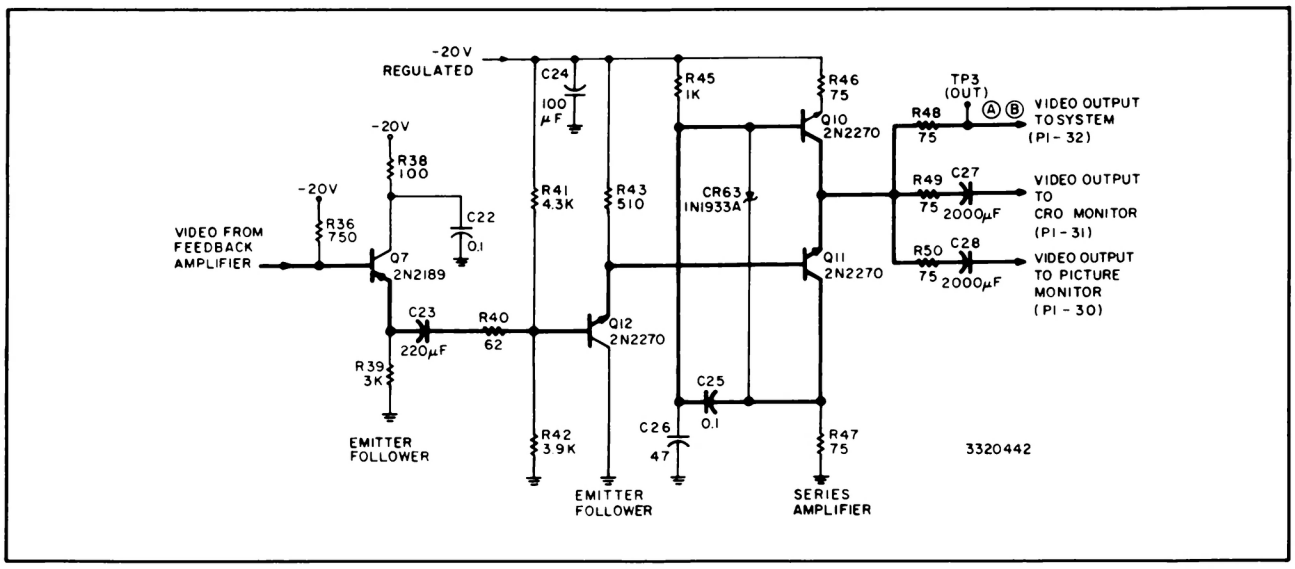
When the control voltage applied to diodes CR61 and CR62 via PEB and NEB is at its maximum value, the diode capacitance is minimum. Thus the total capacitance in the bypass network is also at a minimum and only the higher frequency components of the video signal will be bypassed to ground. As the control voltage decreases, the capacitance of the diodes increases and more and more of the video frequencies at the high end will be bypassed to ground. Since the bypassed frequency components of the video signal are not returned to the base of transistor Q5 as negative feedback, the net result is that of essentially boosting these components.

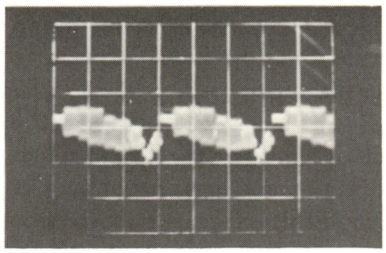
Thus the bypass network has the effect of boosting the higher frequency components of the video signal to compensate for high frequency roll-off inherent in the delay line action. It should be noted however, that the primary purpose of the negative feedback circuit is to maintain the subcarrier frequency component of the video signal at a constant level regardless of the delay presented by delay line DL1. This is important because subcarrier amplitude modulation will cause chroma level changes in the color picture and cannot be tolerated.

Output Driver

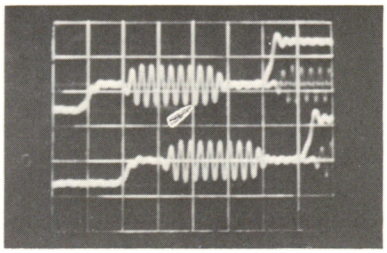
The output driver circuitry, shown in figure 17, consists of emitter follower transistors Q7, Q12 and series amplifier transistors Q10, Q11. The primary purpose of the output driver is to provide the current required to drive three separate output circuits. In addition to providing the required current gain, it is necessary to maintain a flat frequency response over the entire video range. This is accomplished by utilizing an a-c feedback network in the series amplifier circuit.

The video signal at the collector of transistor Q6 in the feedback amplifier circuit is fed directly to the





A. TP3 (OUT), 0.5v/cm.
(20 μsec/cm)



B. Top: TP3 (OUT), 0.2v/cm.
Bottom: Video Input (P1-17),
0.5v/cm.
(1 μsec/cm)

Playback in COLOR ATC mode.

Figure 17—Output Driver Circuit

base of emitter follower transistor Q7. Transistor Q7 is biased into conduction by the negative potential at its base, and the video signal at its emitter is a-c coupled to the base of emitter follower transistor Q12. Resistors R41 and R42 form a voltage divider network between the regulated −20 volts and ground which determines the potential at the base of transistor Q12, and the transistor is biased into conduction by the current withdrawn from its base. When transistor Q12 conducts, the d-c potential at its emitter (approximately −9.5 volts) establishes the operating point of transistor Q11.

The video signal at the base of transistor Q12 also appears at its emitter and is then fed directly to the base of transistor Q11. Transistor Q11 operates in conjunction with transistor Q10 in forming the series amplifier circuit. This circuit is similar to the familiar "totem-pole" amplifier, and its purpose is to provide the amplification required to drive the output circuits while at the same time maintaining a flat frequency response. Additional amplification and gain stabilization is obtained by utilizing an a-c feedback network wherein the video signal appearing at the collector of transistor Q11 is fed back to the base of transistor Q10 via Zener diode CR63 and bypass capacitor C25. Although diode CR63 presents a negligible impedance to the a-c feedback signal, losses occur at the higher video frequencies due to stray capacitance and other factors. To aid in overcoming these losses, the diode is bypassed by 0.1 microfarad capacitor C25.

The primary function of diode CR63 is to establish the operating points of transistors Q10 and Q11 in the following manner: In the series amplifier circuit resistors R46 and R47 are of equal value and, since the same current flows through each resistor, the voltage drop across each is equal. The potential developed across diode CR63 is approximately 12 volts, therefore an 8 volt drop remains to be divided equally between resistors R46 and R47. This results in a potential of −4 volts at the collector of transistor

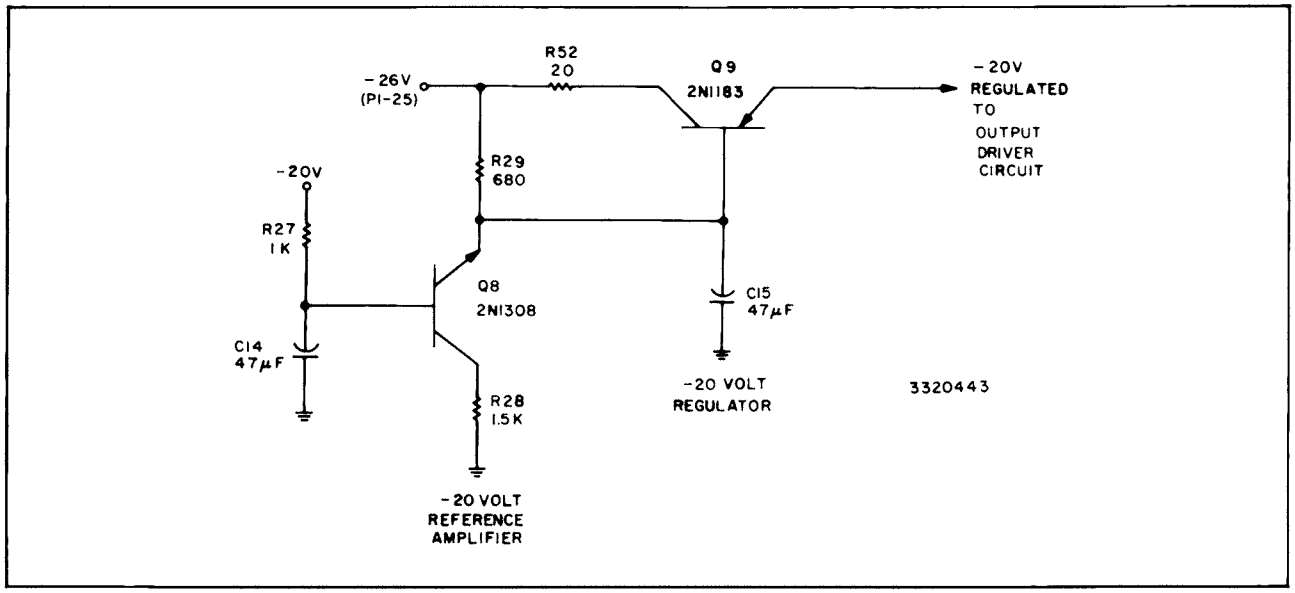


Figure 18— —20 Volt Regulator

Q11 and a potential of −16 volts at the base of transistor Q10. Transistor Q10 is biased into conduction by the current withdrawn from its base, and the potential at its emitter is therefore approximately −16 volts.

The video signal appearing at the collector of transistor Q10 is in phase with the signal at the emitter of transistor Q11, and the resulting output is a balanced video signal having an essentially flat frequency response and an amplitude of 2 volts peak-to-peak. The video output signal is fed to the following three destinations: (1) the chroma separator module (no. 325/C13) via pin 32 of plug P1; (2) the CRO monitor switcher via pin 31 of plug P1; and (3) the picture monitor switcher via pin 30 of plug P1. Test point TP3 (OUT) is provided for convenience in observing the video output signal fed to the chroma separator module (figure 17A). Delay inserted into the tape video path by the color delay module may be observed in figure 17B by comparing the timing of burst in the video output signal (top) with that of burst in the video input signal (bottom).

−20 Volt Regulator

The −20 volt regulator circuit, shown in figure 18, consists of transistors Q8, Q9 and associated circuit components. The function of the regulator circuit is to provide a regulated −20 volt dc potential to the output driver circuit, while at the same time acting as a decoupling network in preventing any current surges which may occur in the driver circuit from excessively loading the −20 volt bus. Current required by the driver circuit is then supplied by the −26 volt dc supply, and the −20 volt biasing potential is obtained from the regulator circuit through the utilization of a −20 volt reference.

Referring to figure 18, the −20 volt potential applied to the base of transistor Q8 biases the transistor into conduction. Therefore a potential of −20 volts appears at the emitter of transistor Q8 and thus at the base of transistor Q9. Transistor Q9 is thereby biased into conduction and its emitter potential is also −20 volts. The potential at the emitter of transistor Q9 is then fed to the output driver circuit. Since the emitter potential of transistor Q9 is clamped at −20 volts by the voltage reference transistor Q8, transistor Q9 actually functions as a variable impedance in series with the output driver circuit. Thus a potential of −20 volts dc is maintained at the emitter of transistor Q9 regardless of normal current variations in the driver circuit.

The −20 volt bus is effectively isolated from the output driver circuit by a decoupling network consisting of two capacitance multipliers in parallel. The capacitance multipliers consist of capacitor C14-transistor Q8 and capacitor C15-transistor Q9 (figure 18), and the value of the equivalent filter capacitor across the −20 volt regulated supply may be calculated as follows:

$$C_D = B_9 [(B_8 \times C14) + C15]$$
$$= B_8 B_9 C14 + B_9 C15$$

Where C_D = decoupling capacitance
B_8 = *beta* of transistor Q8
B_9 = *beta* of transistor Q9

Adjustments

Video Level

Adjust the internal COLOR ATC LEVEL control (potentiometer R13) in the following manner, utilizing a dual-trace *Tektronix Type 535A* oscilloscope or the equivalent:

1. Place the module on a module extender.

2. Connect one probe of the dual-trace oscilloscope to test point TP3 (OUT).

3. Connect the other oscilloscope probe to the video input of the color delay module (at the junction of resistor R14 and the coax cable from pin 17 of plug P1).

4a. In TR-22 machines rotate the FM standards switch (module no. 205) to COLOR STD 1 or 2 position; in TR-3 machines rotate the demodulator output switch (module no. A18) to COLOR position; in TR-4 machines rotate both the demodulator output switch and the modulator switch (module no. A2) to COLOR position.

b. In all machines rotate the selector switch on the ATC delay/output module (no. 223/B11) to ATC OFF position.

5. In TR-22 and TR-4 machines feed a color bar signal (split field with 100% white bar), 3.58 mc subcarrier (4.43 mc subcarrier to machines operating on 625-line standards), and sync to the machine, and operate the machine in STOP mode (MOD/DEMOD). In TR-3 machines, play back a test tape containing 100% white bar, or remove the ATC video out pins (nos. 31 and 15) from the demodulator output module receptacle at the rear of the machine and feed a 1 volt peak-to-peak video signal containing white bar information to the pins.

6. Adjust potentiometer R13 (COLOR ATC LEVEL control) so that the white bar amplitude at test point TP3 (OUT) is equal to that at the video input (junction of resistor R14 and the coax cable from pin 17).

7. Re-insert the module into its receptacle. In TR-3 machines, if the ATC video out pins have been removed from the demodulator output module receptacle (step 5 above) re-insert them into their proper positions at this time.

High Frequency Compensation

High frequency compensation is achieved in the color delay module by adjusting variable capacitor C3. This adjustment is rarely required, but will be necessary if the capacitor is replaced. Test equipment required includes the following:

75-ohm Attenuator
Video Sweep Generator (*Marconi Model 1099* or equivalent)
Dual-Trace Oscilloscope (*Tektronix Type 535A*, or *545A* with CA plug-in, or equivalent)

1. In TR-22 machines, disconnect coax cable from jack J2 of the fixed delay line FDL2 at the rear of the machine, and connect the cable to the output jack of the 75-ohm attenuator.

In TR-3/TR-4 machines, remove the color fixed delay line module (no. 3A3) from the machine and clip a shielded lead between pins 18 and 20 of the fixed delay module receptacle (at the rear of the machine) and the 75-ohm attenuator output jack.

2. Connect the video sweep generator output to the attenuator input jack.

3. Set the attenuator at −8 db.

4. Connect the oscilloscope trigger input to the time base terminal of the sweep generator.

5. Place the color delay module on a module extender, and operate the machine in STOP mode.

6. Connect one of the oscilloscope probes to the video input of the color delay module (at the junction of resistor R14 and the coax cable from pin 17 of plug P1).

7. Connect the other oscilloscope probe to test point TP3 (OUT).

8. Set the sweep generator for a sweep width out to 15 mc, and adjust the generator output for an amplitude of 0.4 volt peak-to-peak as observed on the oscilloscope.

9. Adjust variable capacitor C3 so that the frequency response of the waveform observed at test point TP3 as closely resembles that at the junction of resistor R14 and the video input lead as possible.

10. Remove the test equipment and replace the module(s).

Delay Line Terminations

The delay line termination potentiometers (R2 and R18) have been adjusted for optimum color ATC system performance at the factory, utilizing equipment not generally available in most television studios, and it is extremely unlikely that any readjustment will ever be required. Therefore, unless trouble in the color delay module is traced directly to the delay line, DO NOT CHANGE THE SETTING OF EITHER TERMINATION POTENTIOMETER.

Since component failure within the delay line unit cannot be compensated for by adjusting the termination potentiometers, re-adjustment of a potentiometer is only required when the potentiometer has been inadvertently misadjusted. If misadjustment occurs, the procedure presented below may be followed in re-adjusting the potentiometer for satisfactory color ATC system performance.

NOTE: Before making any adjustments it is advisable to mark the present potentiometer setting by some convenient means (e.g., a scribe mark on the shaft).

Test equipment required for the termination potentiometer re-adjustment includes the following:

75-ohm Attenuator
Video Sweep Generator (*Marconi Model 1099* or equivalent)
Dual-Trace Oscilloscope (*Tektronix Type 535A*, or *545A* with CA plug-in, or equivalent)
Vacuum-tube Voltmeter (*RCA VoltOhmyst* or equivalent)

1. In TR-22 machines, disconnect coax cable from jack J2 of the fixed delay line FDL2 at the rear of the machine, and connect the cable to the output jack of the 75-ohm attenuator.

In TR-3/TR-4 machines, remove the color fixed delay line module (no. 3A3) from the machine and clip a shielded lead between pins 18 and 20 of the fixed delay module receptacle (at the rear of the machine) and the 75-ohm attenuator output jack.

2. Connect the video sweep generator output to the attenuator input jack.

3. Set the attenuator at −8 db.

4. Connect the oscilloscope trigger input to the time base terminal of the sweep generator.

5. Place the color delay module on a module extender, and operate the machine in the STOP mode.

6. Connect one of the oscilloscope probes to the video input of the color delay module (at the junction of resistor R14 and the coax cable from pin 17 of plug P1).

7. Connect the other oscilloscope probe to the sweep generator marker output.

8. Set the sweep generator for a sweep width out to 15 mc, and adjust the generator output for an amplitude of 0.4 volt peak-to-peak as observed on the oscilloscope.

9. Connect the common lead of the vacuum-tube voltmeter to the delay line center (at the junction of 10K-ohm resistor R22 and disc capacitor C11). *Make certain the voltmeter case is insulated from ground.*

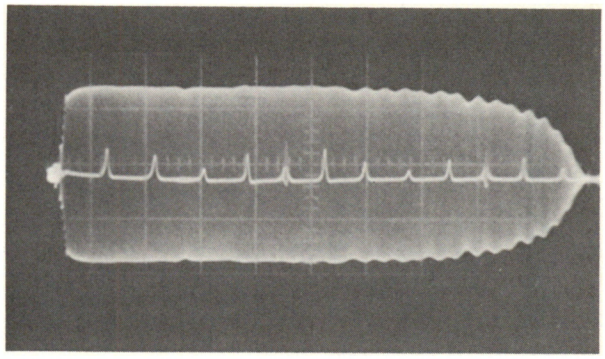


Figure 19—Delay Line Output Waveform with Sweep Generator Input

10. Measure the NEB and PEB voltages at test points TP1 and TP2 to ascertain that they are −2.9 and +2.9 volts dc respectively with respect to the delay line reference voltage. (If they are not, refer to the Color NLA/Error Detector adjustment procedure in the *System Adjustments* section.) Remove the voltmeter after the measurements have been made.

11. Remove the oscilloscope probe from the video input (junction of resistor R14 and the coax cable), and connect it to test point TP3 (OUT).

12. Adjust potentiometer R13 (COLOR ATC LEVEL control) to obtain a sweep signal amplitude of 1 volt peak-to-peak at TP3, as observed on the oscilloscope.

13. While observing the oscilloscope, adjust the 500-ohm terminating potentiometers R2 and R18 to minimize ripples in the response out to 8.0 mc.

14. Adjust variable capacitor C3 to obtain the proper frequency response at TP3. The response should be flat to 8.0 mc (i.e., down by no more than 5% at 8.0 mc), and the signal should be completely cut off at 12.5 mc. (See figure 19.)

NOTE: If the response exhibits excessive ripple, the delay line is faulty. Due to the complexity of repair techniques, the *RCA Service Company* should be consulted if it is determined that the delay line is faulty.

15. Disconnect the sweep generator and attenuator, and re-connect the coax cable to jack J2 of the fixed delay line FDL2 in TR-22 machines or replace the fixed delay line module (no. 3A3) in TR-3/TR-4 machines.

16. Re-adjust potentiometer R13 (COLOR ATC LEVEL) according to the procedure outlined above under *Video Level* adjustment.

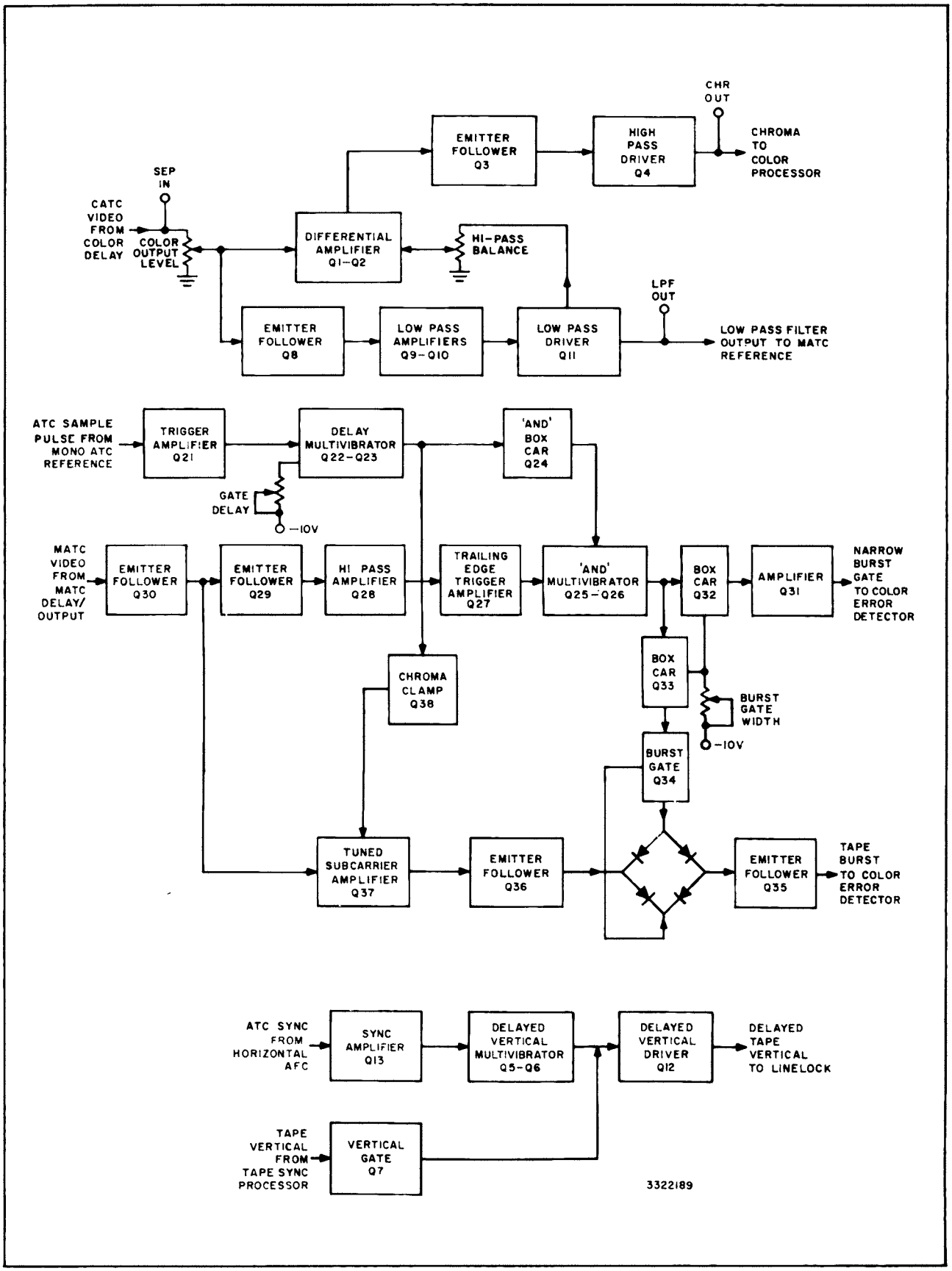


Figure 20—Chroma Separator Module Block Diagram

CHROMA SEPARATOR MODULE, 325/C13

Circuit Description

General

The chroma separator module (no. 325/C13) contains three independent circuits, as shown on the block diagram (figure 20). These are, top to bottom, (1) the chroma separator circuit; (2) the burst separator circuit; and (3) the tape vertical delay circuit.

The purpose of the chroma separator circuit is to separate the low frequency and the high frequency (chroma) components of the color ATC video signal so that they may be independently processed before being recombined. The separated high frequency (chroma) signal is fed to special processing circuitry in the color processor module. Special processing circuitry for the high frequency signal is required because the monochrome processing amplifier circuits will clamp out the burst signal and the black clipper will remove all signal components below black level. The low frequency signal is fed to the monochrome processing circuits in the video control module via the monochrome ATC reference module and the bypass relays. In the monochrome ATC reference module, sync is separated from the low frequency signal components and fed to sync processing circuits in the horizontal AFC module via the chroma separator module and the bypass relays. In the chroma separator module, separated sync is utilized as a trigger in the tape vertical delay circuitry.

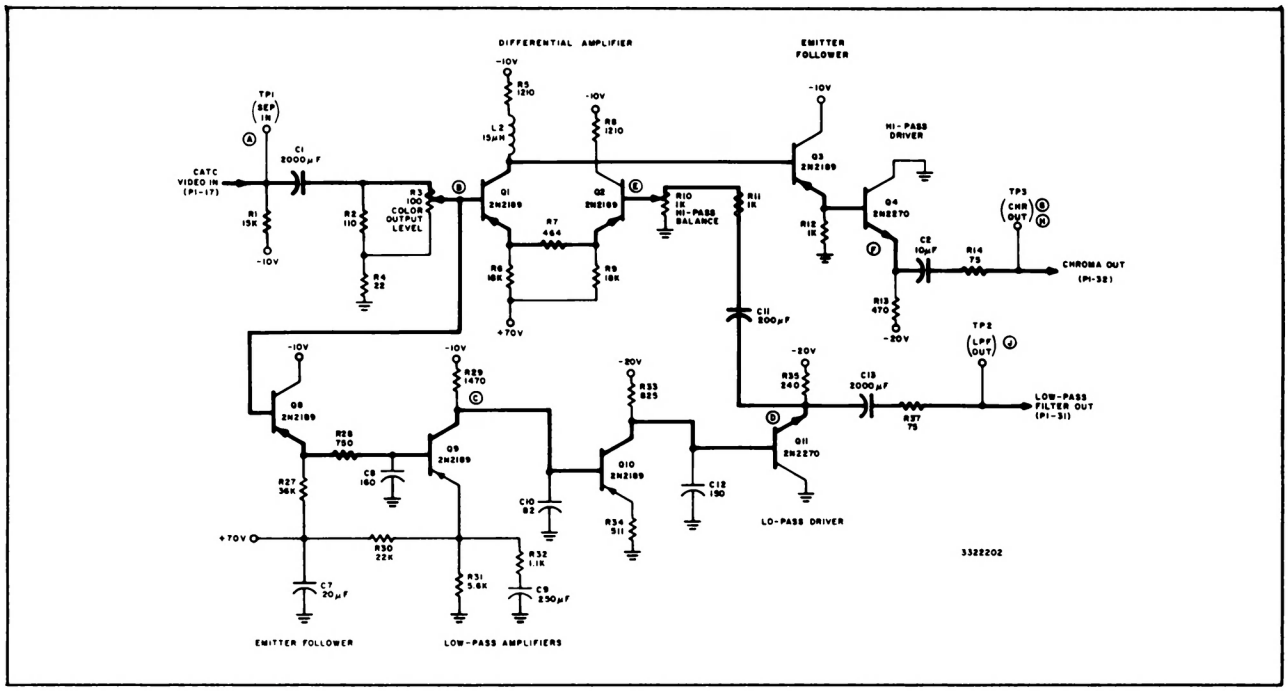
Controls in the chroma separator circuit consist of the COLOR OUTPUT LEVEL and HIGH-PASS BALANCE potentiometers. The COLOR OUTPUT LEVEL potentiometer is set for unity gain of the low pass signal from the input of the chroma separator circuit to the output, while the HIGH-PASS BALANCE potentiometer is utilized in cancelling all low frequency information in the chroma signal.

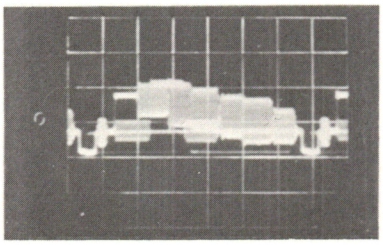
The burst separator circuitry utilizes a diode bridge (quad) in separating burst from the monochrome ATC video signal. The quad is controlled by "rough" burst gating pulses derived from the trailing edge of monochrome ATC sync, and the trailing edge of sync is extracted from the video signal by opening an 'AND' gate just before the trailing edge occurs. Information utilized in opening the 'AND' gate is obtained from the ATC sample pulse which precedes the trailing edge of sync by a known amount and which has been previously gated to exclude 9H information. The rough burst gating pulse circuitry also provides a narrow burst gating pulse. The narrow burst gating pulse is delayed slightly with respect to the rough burst gating pulse and is made narrower so that it actually occurs within the rough burst gating interval.

Burst separated from the monochrome ATC video signal and the narrow burst gating pulse are both fed to the color error detector module where the narrow burst gating pulse removes a segment from the center of the separated burst signal for the development of phase sample pulses in a burst logic circuit. The BURST GATE WIDTH potentiometer controls the width of the rough and narrow burst gating pulses simultaneously, and is utilized in adjusting the width of the rough burst gating pulse to its optimum value.

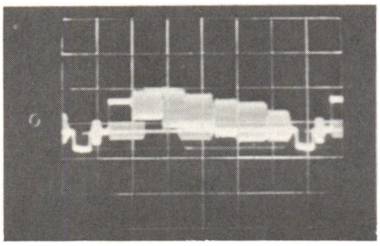
The low frequency component of the color ATC video signal obtained from the chroma separator circuit is fed to the monochrome ATC reference module, where composite sync is separated and fed back to the tape vertical delay circuit in the chroma separator module. The tape vertical signal from the tape sync processor module is also fed to the tape vertical delay circuit. The tape vertical signal is generated from tape sync obtained from the demodulator output module, and therefore precedes color ATC sync by approximately 11 microseconds due to delays in the color ATC system. In the tape vertical delay circuit, the tape vertical signal from the tape sync processor module opens a gate which allows a monostable multivibrator to be triggered. After the gate has been opened the monostable multivibrator will be triggered by the next edge which occurs, and this edge is the leading edge of the second vertical sync pulse. The output of the monostable multivibrator will then be a pulse having a duration of approximately 300 microseconds and a leading edge timed with color ATC sync which in turn is delayed 11 microseconds with respect to the demodulator output sync. Therefore the delayed vertical pulse will be approximately aligned with the reference vertical pulse, since the horizontal phasing controls are normally set to align the output of the machine with reference sync.

The effect of the tape vertical delay circuit, therefore, is to produce a vertical rate pulse which is delayed by an amount equal to the total delay inserted into the tape video path in the color ATC system so that the signals derived from the tape vertical signal in the lock sense and TVA circuits of the pixlock servo system will be well within the "lock-in" range required for proper operation of these circuits. The delayed tape vertical signal is fed to the linelock module where it is utilized in the lock sense and TVA circuits when the machine is operating in the color ATC mode. If the machine is not operating in the color ATC mode, the tape vertical delay circuitry is bypassed and the tape vertical signal is fed directly from the tape sync processor module to the linelock module.

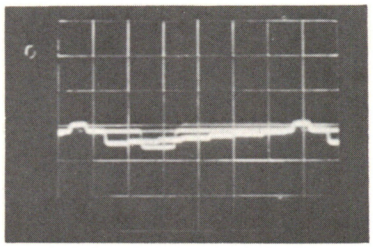




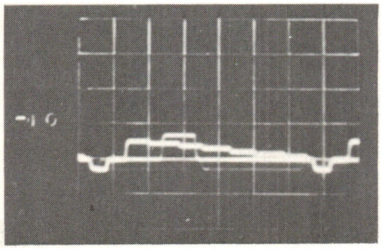
A. TP1 (SEP IN), 0.5v/cm.



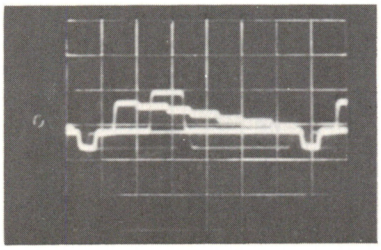
B. Q1 base, 0.5v/cm.



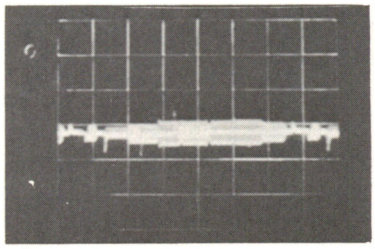
C. Q9 collector, 2v/cm.



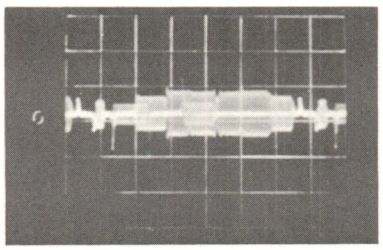
D. Q11 emitter, 2v/cm.



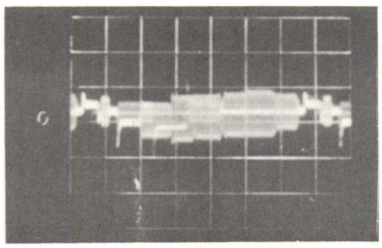
E. Q2 base, 0.5v/cm.



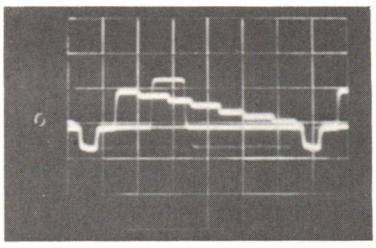
F. Q4 emitter, 2v/cm.



G. TP3 (CHR OUT), 0.5v/cm. (R10 Correctly Adjusted)



H. TP3 (CHR OUT), 0.5v/cm. (R10 Incorrectly Adjusted)



J. TP2 (LPF OUT), 0.5v/cm.

Machine in STOP mode (back-to-back signal). All sweep times 10 μsec/cm.

Figure 21—Chroma Separator Circuit

Chroma Separator Circuit

The chroma separator circuit (figure 21) separates the high frequency components of the tape video signal (chroma) from the low frequency components. This separation is necessary because the chroma signal cannot be processed properly in the monochrome processing amplifier circuits and must therefore be processed by special circuitry in the color processor module (no. 231/C15) of the color ATC system. The low frequency components of the tape video signal are fed via COLOR/BYPASS relay K21A and MONO/BYPASS relay K11A to the monochrome processing amplifier circuits and to the sync separator circuit in the monochrome ATC reference module (no. 226/B14). From the ATC reference module the separated signal is fed back to the vertical delay circuit in this module where it is utilized in controlling the delay of the tape vertical signal.

The input to the chroma separator circuit is the tape video signal from the color delay module (no. 324/C12). The tape video signal is fed to the module at pin 17 of plug P1, and may be observed at test point TP1 (SEP IN). (See figure 21A.) Resistors R2-R4 and potentiometer R3 (COLOR OUTPUT LEVEL) combine to form a 75-ohm input impedance. Potentiometer R3 is utilized in setting the level of the tape video signal fed simultaneously to the bases of transistors Q1 and Q8 (figure 21B). (The correct method of adjusting potentiometer R3 is outlined below under *Adjustments.*)

Transistors Q1 and Q2 combine to form a differentiating amplifier circuit whose operation is described below. Transistor Q8 functions as an emitter follower in providing a high input impedance and thus isolating the low-pass filter and amplifier circuits from the input video circuit. The low-pass filter circuit consists of three resistance-capacitance networks (R28-C8, R29-C10, and R33-C12) which are isolated from each other by transistors Q9 and Q10. Transistors Q9 and Q10 (figure 21C) also provide a low frequency gain of approximately 2, so that a 1 volt peak-to-peak output signal may be obtained when the COLOR OUTPUT LEVEL potentiometer is set at the center of its range. Emitter follower transistor Q11 provides the current gain required to drive the low frequency output signal, and the signal at the emitter of Q11 (figure 21D) is coupled back to the differential amplifier in addition to being fed to the low frequency output circuit.

As mentioned above, transistors Q1 and Q2 form the differential amplifier circuit. The signal fed to the base of transistor Q1 from the center-arm of potentiometer R3 is the complete video signal, containing high frequency signal components (chroma) as well as low frequency components (figure 21B). However, the signal applied to the base of transistor Q2 from the center-arm of potentiometer R10 contains only the low frequency components remaining after the high frequency components have been filtered out (figure 21E). Since the low frequency signal components have been subjected to a 360-degree phase shift by the low-pass amplifier transistors Q9 and Q10, the low frequency components appearing in the essentially common emitter circuit of transistors Q1 and Q2 will be in phase. Therefore, a change in amplitude of the low frequency signal components fed to the base of transistor Q1 will be followed by a proportional amplitude change at the emitter of Q1 and no amplification of the low frequency components will result. Thus only the high frequency signal components will be amplified by transistor Q1. Potentiometer R10 (HI-PASS BALANCE) is utilized in adjusting the level of the low frequency signal components fed to the base of transistor Q2 so that the amplitudes of the low frequency components at the emitter of Q2 will equal those of the low frequency components appearing in the emitter circuit of transistor Q1. (The correct method of adjusting balance potentiometer R10 is presented below under *Adjustments.*)

Peaking coil L2, in the collector circuit of transistor Q1, prevents roll-off of the high frequency response due to the action of resistor R5 and the input capacitance of transistor Q3. The high frequency video signal components are thus fed directly to the base of emitter follower transistor Q3, which operates in conjunction with emitter follower transistor Q4 in providing the current gain required to drive the high frequency output signal (chroma). The chroma signal at the emitter of driver transistor Q4 (figure 21F) is fed via pin 32 of plug P1 to the color processor module where the required processing is accomplished. Test point TP3 (CHR OUT) is provided for convenience in observing the output chroma signal. Figure 21G shows the chroma output at test point TP3 with HI-PASS BALANCE potentiometer R10 correctly adjusted, while figure 21H shows the chroma output with potentiometer R10 incorrectly adjusted.

The low-pass filter output from transistor Q11 may be observed at test point TP2 (LPF OUT), and is shown in figure 21J. The output is fed via pin 31 of plug P1 to the COLOR (normally open) contact of COLOR/BYPASS relay K21A. When the machine is operated in the normal color ATC or non-phased color (NPC) mode, the COLOR/BYPASS relay (K21A) and the MONO/BYPASS relay (K11A) are energized and the low frequency component signal is fed to both the sync separator circuit in the

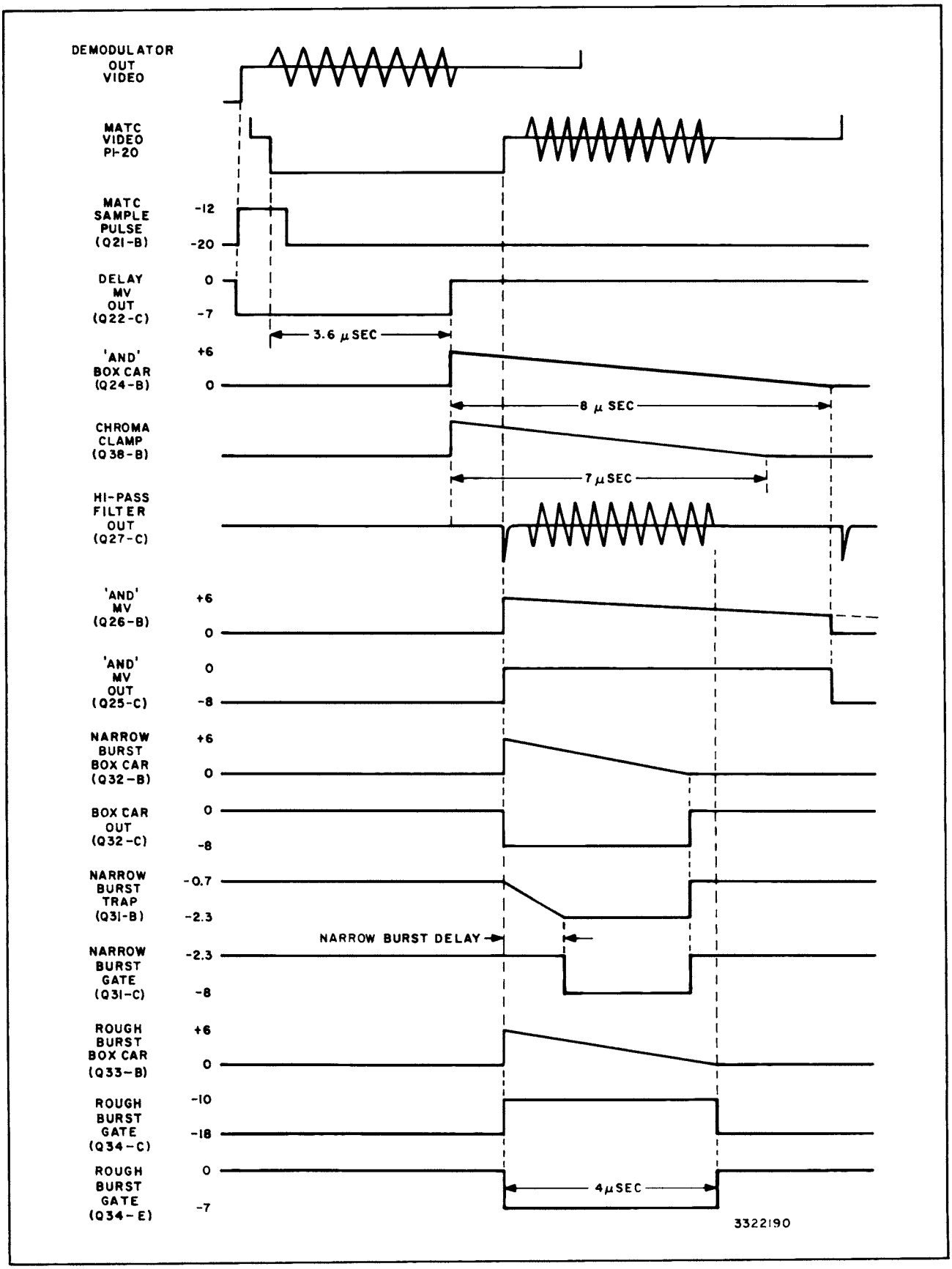


Figure 22—Burst Gate Timing Diagram

monochrome ATC reference module and the monochrome processing amplifier circuits. Composite sync separated from the low frequency components of the video signal is then fed back to the tape vertical delay circuit in this module. (See *Tape Vertical Delay* discussion below.)

Burst Separator

A. Sample Pulse Delay

As shown on the timing diagram (figure 22), the leading edge of the ATC sample pulse is timed to the trailing edge of sync separated from the tape video signal in the demodulator output module (no. 303A/A18). The derivation of the ATC sample pulse takes place in the monochrome ATC error detector module (no. 225/B13) and the pulse is then fed via the monochrome ATC reference module (no. 226/B14) to the chroma separator module at pin 26 of plug P1.

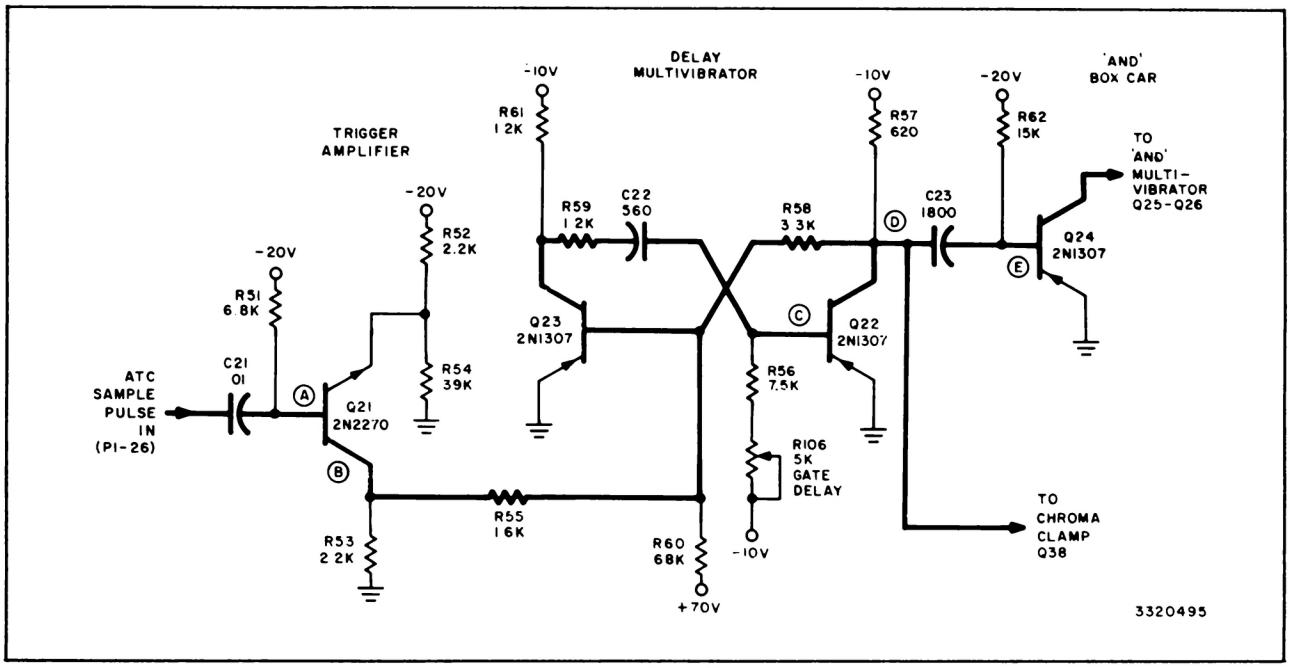
The positive-going sample pulse appearing at pin 26 is fed to the base of trigger amplifier transistor Q21 (figure 23A). A potential of approximately −19 volts is applied to the emitter of transistor Q21 from the divider network consisting of resistors R52 and R54 and, since this potential is positive with respect to its base potential, the transistor is normally cut off. The positive-going (leading) edge of the ATC sample pulse appearing at the base of transistor Q21 drives the transistor into conduction, and a negative-going pulse then appears at its collector (figure 23B). This pulse is applied as a triggering pulse to the base of transistor Q23 in the delay multivibrator circuit.

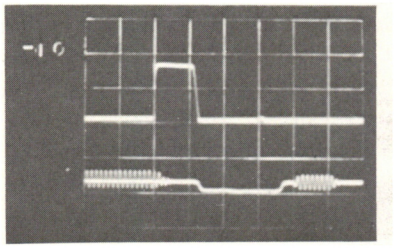
Transistors Q22-Q23 and associated circuit components form the monostable delay multivibrator. In the multivibrator stable state transistor Q22 is biased into saturation and transistor Q23 is cut off. The potential at both the base and collector of transistor Q22 is then approximately ground, and the collector potential of transistor Q23 is −10 volts. Therefore, due to capacitor C22, the potential at the base of transistor Q22 is approximately 10 volts positive with respect to that at the collector of transistor Q23. The negative-going (leading) edge of the pulse fed to the base of transistor Q23 drives Q23 into saturation and its collector potential immediately rises to ground. However, since the voltage across capacitor C22 cannot change instantaneously, the base potential of transistor Q22 remains positive with respect to the collector potential of transistor Q23 and thus is positive with respect to ground. This drives transistor Q22 into cut-off and, due to the divider network consisting of resistors R57, R58, and R60 between +70 volts and −10 volts, the collector potential of Q22 falls to approximately −7 volts.

At the instant transistor Q23 is driven into saturation the multivibrator timed cycle (unstable state) begins. The base potential of transistor Q22 then decreases toward −10 volts as capacitor C22 discharges through resistor R56 and potentiometer R106 (figure 23C). When the base potential of transistor Q22 becomes slightly negative with respect to ground, transistor Q22 is biased into saturation and its collector potential rises to ground. Transistor Q23 is then biased into cut-off by the positive potential applied to its base from the divider network consisting of resistors R58 and R60 between +70 volts and ground, and the multivibrator timed cycle ends.

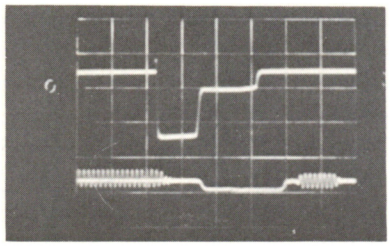
The timed cycle of the delay multivibrator is determined by the values of capacitor C22, resistor R56, and potentiometer R106 returned to −10 volts. Potentiometer R106 (GATE DELAY) is adjusted so that its setting, in conjunction with the values of capacitor C22 and resistor R56, results in a multivibrator timed cycle of approximately 4 microseconds. Therefore the width of the negative-going pulse at the collector of transistor Q22 is approximately 4 microseconds (figure 23D). Since the delay multivibrator is in effect triggered by the positive-going (leading) edge of the ATC sample pulse, the positive-going (trailing) edge of the pulse output at the collector of transistor Q22 occurs approximately 4 microseconds later and thus the desired delay is attained. (See timing diagram, figure 22.) The setting of potentiometer R106 (GATE DELAY) is fairly critical since proper operation of the burst separator circuitry requires the positive-going edge of the multivibrator output pulse to occur during the ATC sync interval, between the point where video head switching occurs (approximately 1/3 in from the leading edge of sync) and the positive-going trailing edge of sync. A procedure for properly adjusting potentiometer R106 is presented below under *Adjustments*.

The negative-going pulse at the collector of delay multivibrator transistor Q22 is fed to the boxcar circuit of transistor Q24, and to chroma clamp transistor Q38. Transistor Q24 is normally saturated by the current withdrawn from its base, and its collector is then at ground potential. Since transistor Q24 is normally saturated, the negative-going leading edge of the delay multivibrator output pulse has no effect on the transistor; however, the positive-going trailing edge of the pulse drives the transistor into cut-off. At the instant transistor Q24 is driven into cut-off, its base potential rises to approximately +6 volts with respect to ground due to the fact that the voltage across capacitor C23 cannot change instantaneously. Then, as capacitor C23 discharges through resistor R62 toward −20 volts the base potential of transistor Q24 also goes in a negative direction (figure 23E).

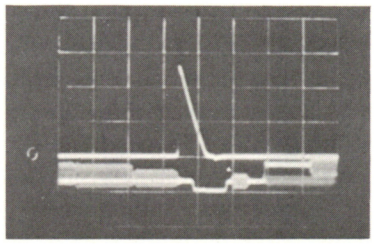




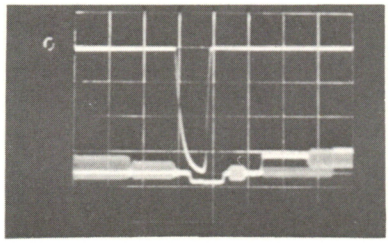
A. Top: Q21 base, 5v/cm.
Bottom: ATC Video (P1-20), 1v/cm.
(2 μsec/cm)



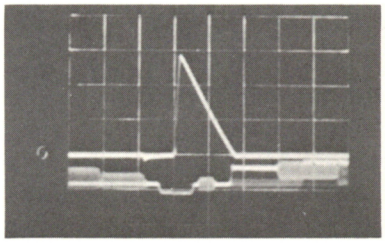
B. Top: Q21 collector, 2v/cm.
Bottom: ATC Video (P1-20), 1v/cm.
(2 μsec/cm)



C. Top: Q22 base, 2v/cm.
Bottom: ATC Video (P1-20), 1v/cm.



D. Top: Q22 collector, 2v/cm.
Bottom: ATC Video (P1-20), 1v/cm.



E. Top: Q24 base, 2v/cm.
Bottom: ATC Video (P1-20), 1v/cm.

Machine in STOP mode (back-to-back signal). All sweep times 5 μsec/cm unless otherwise noted.

Figure 23—Sample Pulse Delay

When the base potential of transistor Q24 goes slightly negative with respect to ground, the transistor becomes saturated once again.

The operation of the box car circuit would normally produce a negative-going pulse, having a width determined by the rate at which capacitor C23 discharges through resistor R62 toward −20 volts, at the collector of transistor Q24. However, the collector of transistor Q24 is resistance coupled to the collector of trigger amplifier transistor Q27, whose operation is described below, and the collector potential of Q24 is therefore determined by the condition of Q27. It is sufficient to state here that due to the values of R62 and C23 transistor Q24 is cut off for an interval of approximately 8 microseconds, and the beginning of the cut-off interval is timed to the positive-going (trailing) edge of the delay multivibrator output pulse. The beginning of the cut-off interval of transistor Q24 is thus delayed 4 microseconds with respect to the leading edge of the ATC sample pulse (or is delayed approximately 3.6 microseconds with respect to the negative-going leading edge of ATC sync). (See timing diagram, figure 22.)

B. High-Pass Filter and Trigger Amplifier

The ATC video signal, obtained from the monochrome ATC delay/output module (no. 223/B11), is fed to the chroma separator module at pin 20 of plug P1 (figure 24A) and is then coupled to the base of emitter follower transistor Q30 (figure 24B). The base potential of transistor Q30 is established at approximately −4 volts by the divider network consisting of resistors R75 and R76, and the transistor is biased into conduction by the current withdrawn from its base. The high input impedance of transistor Q30 provides effective isolation, and its low output impedance allows the transistor to act as a source of current for driving the high-pass amplifier and subcarrier amplifier circuits which follow.

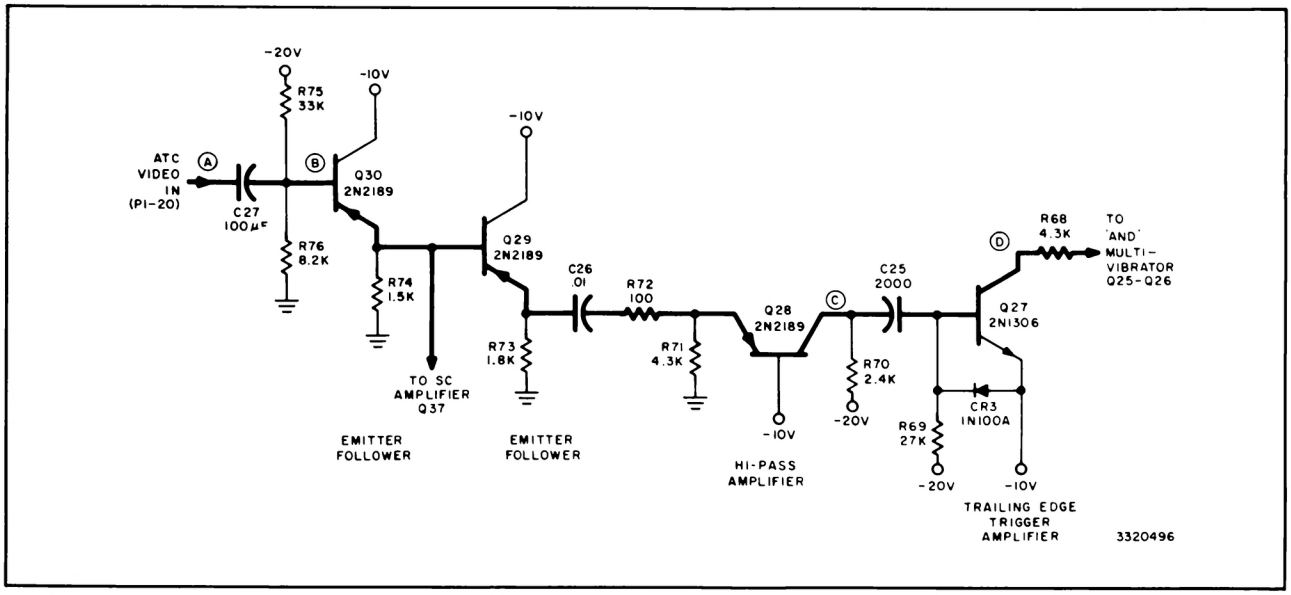
The video signal at the emitter of transistor Q30 is fed directly to the base of transistor Q29 and also to the subcarrier amplifier circuitry. Transistor Q29, functioning as an emitter follower, provides a high input impedance which effectively isolates the high-pass filter and amplifier circuits from the subcarrier amplifier. Capacitor C26 and resistor R72 in series comprise a high-pass network which provides the high frequency components of the video signal with a low impedance path to common base amplifier transistor Q28. Transistor Q28 functions as a voltage amplifier, and the signal at its collector (figure 24C) is fed to trailing edge trigger amplifier transistor Q27.

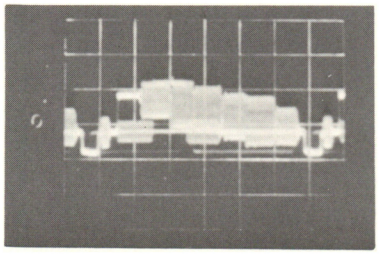
Diode CR3 in the circuit of trigger amplifier transistor Q27 is forward biased and, since the diode contact potential is approximately 0.2 volt, the base potential of Q27 is approximately −10.2 volts. Transistor Q27 is thus normally cut off by the contact potential of diode CR3. During normal circuit operation then, transistor Q27 is cut off and 'AND' box car transistor Q24 is saturated (see *Sample Pulse Delay* discussion above). Under these conditions the collector of transistor Q27 is clamped at ground potential. Negative-going excursions of the high frequency video signal components fed to the base of transistor Q27 have no effect on the transistor operation, however positive-going excursions drive the transistor into conduction. When transistor Q27 is driven into conduction and box car transistor Q24 is saturated, current flowing in the collector circuit of transistor Q27 is drawn from transistor Q24 and a series of negative-going pulses, timed to the positive-going edges of the high frequency ATC video signal components, appears at the collector of Q27 (figure 24D). When transistor Q27 is driven into conduction and box car transistor Q24 is cut off, current flowing in the collector circuit of Q27 is drawn from transistor Q25 in the 'AND' multivibrator circuit, thus biasing Q25 into conduction (see *'AND' Multivibrator* discussion and figure 25 below).

C. 'AND' Multivibrator and Burst Gating Circuits

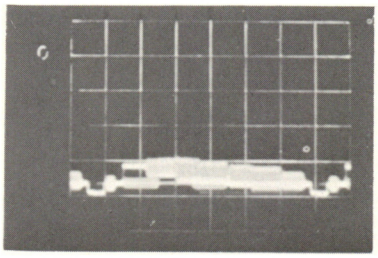
Transistors Q25-Q26 and associated circuit components form the monostable 'AND' multivibrator (figure 25). In the multivibrator stable state, transistor Q26 is biased into saturation and transistor Q25 is cut off. The multivibrator is triggered into its unstable state when a negative potential appears at the base of transistor Q25, and the application of this negative potential is controlled by the output from trailing edge trigger amplifier transistor Q27 in conjunction with the gating action of 'AND' box car transistor Q24.

In the circuit description above, it was stated that a negative-going pulse appears at the collector of transistor Q27 whenever a positive-going excursion of the high frequency component of the video signal occurs, and that the collector of Q27 is at ground potential when Q27 is cut off. It was also stated that the collector of transistor Q24 is at ground potential when Q24 is saturated. Therefore, during the saturation interval of transistor Q24 the base of transistor Q25 is clamped at ground potential and negative-going pulses at the collector of transistor Q27 will have no effect on the 'AND' multivibrator. When transistor Q24 is driven into cut-off, transistor Q25 remains held in cut-off by the ground potential at the collector of transistor Q27 until a negative-going pulse appears at the collector of Q27. Thus the first negative-going pulse at the collector of transistor Q27 after transistor Q24 has been cut off also appears

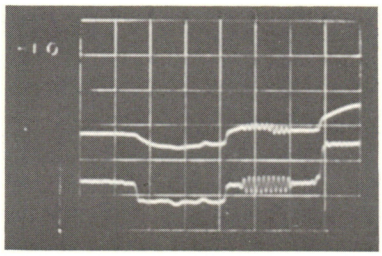




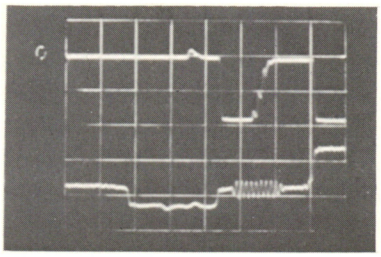
A. ATC Video (P1-20), 0.5v/cm.
(10 μsec/cm)



B. Q30 base, 1v/cm.
(10 μsec/cm)



C. Top: Q28 collector, 2v/cm.
Bottom: ATC Video (P1-20),
0.5v/cm.
(2 μsec/cm)



D. Top: Q27 collector, 5v/cm.
Bottom: ATC Video (P1-20),
0.5v/cm.
(2 μsec/cm)

Machine in STOP mode (back-to-back signal).

Figure 24—High-Pass Filter and Trigger Amplifier

at the base of transistor Q25. The negative-going pulse then drives transistor Q25 into saturation and the multivibrator timed cycle (unstable state) begins. As shown on the timing diagram (figure 22), the negative-going pulse which drives transistor Q25 into saturation is timed to the positive-going (trailing) edge of ATC sync. It should also be noted that once the multivibrator timed cycle begins, the multivibrator cannot be re-triggered until it has completed that cycle. Therefore, since transistor Q24 is returned to its saturated state before the end of the normal multivibrator timed cycle (as explained below), no further triggering pulses will appear at the base of transistor Q25 until the next line occurs (figure 25A).

In the 'AND' multivibrator stable state, transistor Q26 is saturated and its base and collector are at ground potential. Simultaneously, transistor Q25 is cut off and its collector potential is approximately −8 volts. Thus the base of transistor Q26 is approximately 8 volts positive with respect to the collector of transistor Q25. When transistor Q25 is driven into saturation its collector potential immediately rises to ground and, since the voltage across capacitor C24 cannot change instantaneously, the potential at the base of transistor Q26 goes positive with respect to ground. This action cuts off transistor Q26 and begins the multivibrator timed cycle.

As capacitor C24 discharges through resistor R67 the base potential of transistor Q26 goes toward −10 volts (figure 25B). Normally, when the base potential of transistor Q26 has reached a level which is slightly negative with respect to ground due to capacitor C24 discharging through resistor R67, the transistor would be biased into conduction once again and the timed cycle would end. However, before capacitor C24 has discharged to the forward biasing level of transistor Q26, transistor Q24 is returned to its saturated state. Transistor Q25 is then cut off by the ground potential applied to its base, thus causing transistor Q26 to be driven into saturation, and the multivibrator timed cycle is prematurely ended. (See timing diagram, figure 22.) The width of the resulting positive-going pulse which appears at the collector of transistor Q25 (figure 25C) is therefore determined primarily by the length of time that transistor Q24 remains cut off after the trailing edge of ATC sync has occurred. Since transistor Q25 is driven into saturation by a pulse derived from the positive-going trailing edge of ATC sync, the positive-going (leading) edge of the multivibrator output pulse is also timed to the trailing edge of ATC sync.

The 'AND' multivibrator output pulse is fed to parallel box car circuitry, as shown in figure 25. Box car transistor Q32, in the narrow burst gating pulse circuit, is normally biased into saturation and its base and collector are then at ground potential. The positive-going (leading) edge of the 'AND' multivibrator output pulse drives transistor Q32 into cut-off and the collector potential of Q32 falls to approximately −8 volts. At the instant transistor Q32 is driven into cut-off, capacitor C31 begins to discharge through resistor R83 to the potential across capacitor C33 which in turn is determined by the average current flowing through potentiometer R84. As capacitor C31 discharges through resistor R83 the potential at the base of transistor Q32 goes in a negative direction (figure 25D) and, when the base potential of Q32 becomes slightly negative with respect to ground, the transistor is biased into saturation once again. Thus the signal at the collector of box car transistor Q32 is a negative-going pulse (figure 25E), having an amplitude of approximately 8 volts and a width which is determined by the amplitude of the 'AND' multivibrator output pulse in conjunction with the discharge rate of capacitor C31.

Similarly, box car transistor Q33 in the "rough" burst gating pulse circuit also produces a negative-going pulse at its collector. In this case, the width of the negative-going pulse at the collector of transistor Q33 is determined by the amplitude of the 'AND' multivibrator output pulse in conjunction with the rate at which capacitor C32 discharges through resistor R85 toward the voltage across capacitor C33 (figures 25H and 25J). As mentioned in the above paragraph, the voltage across capacitor C33 is determined by the average current flowing through potentiometer R84. Since potentiometer R84 is common to both box car circuits, the width of both the pulse at the collector of transistor Q32 and the pulse at the collector of transistor Q33 depends upon the potentiometer setting; thus as the potentiometer is adjusted, the width of both pulses will vary simultaneously. It should be noted that since the value of capacitor C31 is less than that of capacitor C32, the cut-off interval of transistor Q32 is shorter than that of transistor Q33. As a result of the unequal cut-off intervals of transistors Q32 and Q33, the pulse at the collector of Q32 is narrower than the pulse at the collector of Q33. Both gating pulses, however, have negative-going leading edges which are timed to the positive-going leading edge of the 'AND' multivibrator output pulse.

When narrow burst box car transistor Q32 is saturated its collector is at ground potential and diode CR4 is forward biased. Due to the contact potential of diode CR4 and transistor Q32 the base potential of transistor Q31 is then −0.7 volt and, since the emitter potential of Q31 is established at −2.3 volts by the divider network consisting of resistors R78 and R80, the transistor is cut off. When the positive-going leading edge of the 'AND' multivibrator output pulse drives transistor Q32 into cut-off its collector potential immediately falls to −8 volts. Since the potential across capacitor C30 (−0.7 volt) cannot change instantaneously, diode CR4 is cut off. Capacitor C30 then begins to charge through resistor R81, and the base potential of transistor Q31 falls toward −10 volts. As the potential at the base of transistor Q31 goes negative with respect to −2.3 volts, the transistor begins to conduct and its base is clamped at −2.3 volts. At the end of the box car timed period, transistor Q32 goes back into saturation and its collector returns to ground potential.

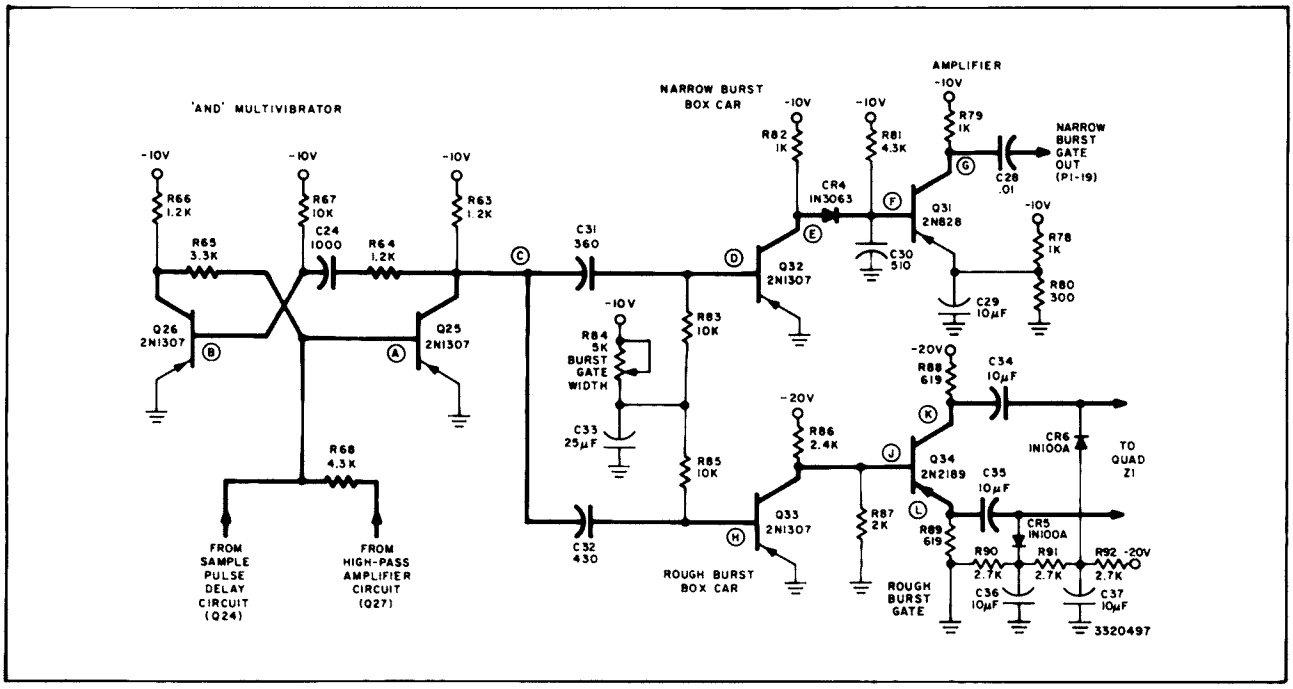


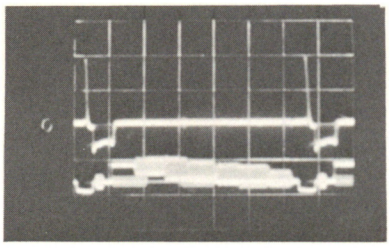
Figure 25—'AND' Multivibrator and Burst Gating Circuits

Diode CR4 is then forward biased once again and, as capacitor C30 discharges rapidly through CR4 and transistor Q32, the base potential of transistor Q31 rises to −0.7 volt and the transistor is cut off (figure 25F).

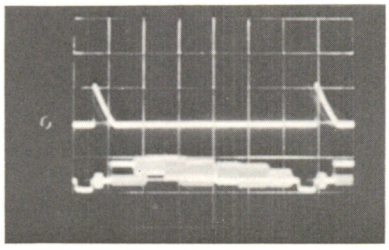
Therefore diode CR4, capacitor C30, and resistor R81 form a trapezoid generator circuit, and the resulting pulse output at the collector of transistor Q31 has a positive-going leading edge which is delayed with respect to the leading edge of the gating pulse at the collector of transistor Q33. The actual delay (approximately 1 microsecond) is determined by the values of capacitor C30 and resistor R81 returned to −10 volts. (See timing diagram, figure 22.) The positive-going pulse at the collector of transistor Q31 (figure 25G) is designated the narrow burst gating pulse and is fed to the color error detector module (no. 326/C14) where it is utilized in the logic circuits which develop the phase sample pulse.

The negative-going pulses at the collector of rough burst box car transistor Q33 are fed directly to the base of rough burst gate transistor Q34 (figure 25J). During the interval between negative-going pulses the collector of transistor Q33 is at ground potential and, since this potential is applied directly to the base of transistor Q34, transistor Q34 is cut off. When a negative-going pulse appears at the collector of transistor Q33, and thus at the base of transistor Q34, transistor Q34 is driven into conduction. The amplitude of the negative-going pulse is limited by the action of the voltage divider network consisting of resistors R86 and R87 so that transistor Q34 cannot be driven into saturation. Therefore, each negative-going pulse appearing at the collector of transistor Q33 produces a positive-going pulse at the collector of burst gate transistor Q34 (figure 25K) and a negative-going pulse at the emitter of Q34 (figure 25L). The positive- and negative-going pulses at the collector and emitter respectively of transistor Q34 are designated the rough burst gating pulses, and are coupled to quad Z1 where they control the quad diodes. The rough burst gating pulse width may be varied by adjusting potentiometer R84 (BURST GATE WIDTH), as explained above, and the correct procedure for making this adjustment is outlined below under *Adjustments*.

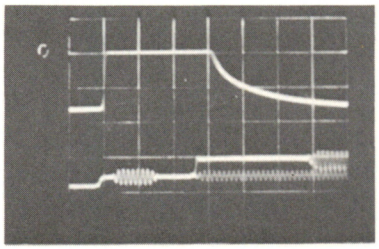
Resistors R90, R91, and R92 in conjunction with diodes CR5 and CR6 form a voltage divider which functions as a level-setting network in establishing an 'off' bias of approximately 8 volts across quad Z1 during the interval between gating pulses. The amplitude of the positive- and negative-going gating pulses is determined by the drive applied to the base of transistor Q34, and the drive is in turn established by the divider network consisting of resistors R86 and R87. The drive applied to transistor Q34 in conjunction with the levels obtained from the level setting network results in a gating pulse overlap of approximately 9 volts. The overlap potential is utilized in developing the current required for proper operation of the quad, as explained below.



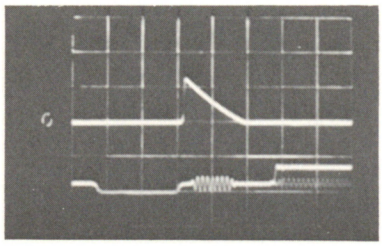
A. Top: Q25 base, 0.5v/cm.
Bottom: ATC Video (P1-20), 1v/cm.
(10 μsec/cm)



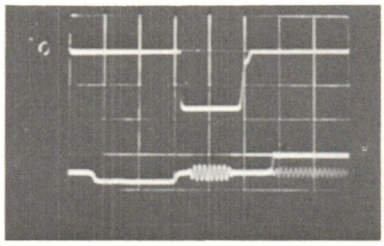
B. Top: Q26 base, 5v/cm.
Bottom: ATC Video (P1-20), 1v/cm.
(10 μsec/cm)



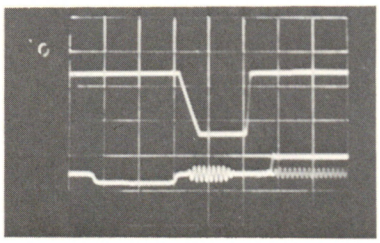
C. Top: Q25 collector, 5v/cm.
Bottom: ATC Video (P1-20), 1v/cm.



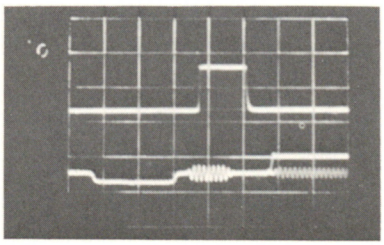
D. Top: Q32 base, 5v/cm.
Bottom: ATC Video (P1-20), 1v/cm.



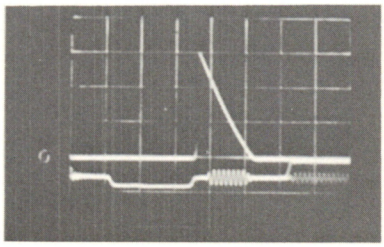
E. Top: Q32 collector, 5v/cm.
Bottom: ATC Video (P1-20), 1v/cm.



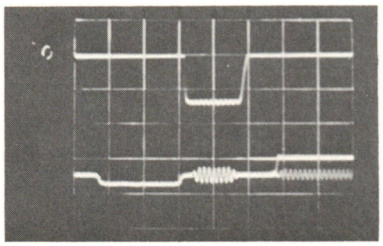
F. Top: Q31 base, 1v/cm.
Bottom: ATC Video (P1-20), 1v/cm.



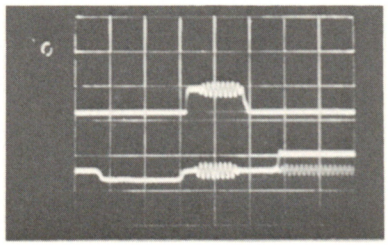
G. Top: Q31 collector, 5v/cm.
Bottom: ATC Video (P1-20), 1v/cm.



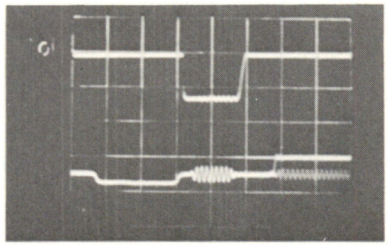
H. Top: Q33 base, 2v/cm.
Bottom: ATC Video (P1-20), 1v/cm.



J. Top: Q34 base, 5v/cm.
Bottom: ATC Video (P1-20), 1v/cm.



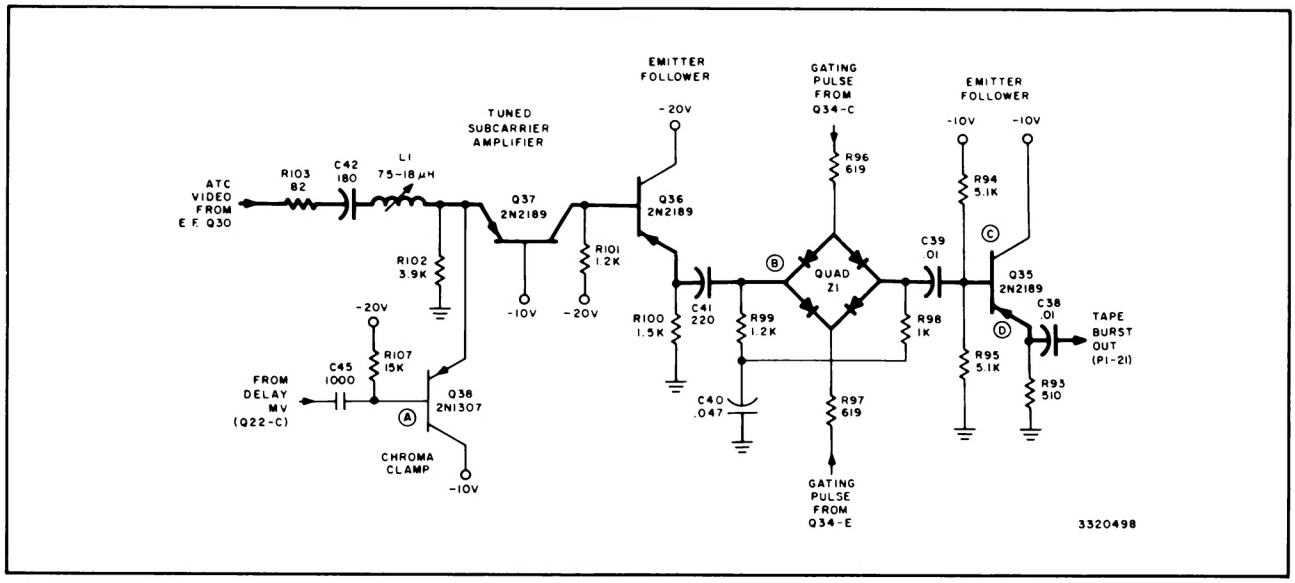
K. Top: Q34 collector, 10v/cm.
Bottom: ATC Video (P1-20), 1v/cm.

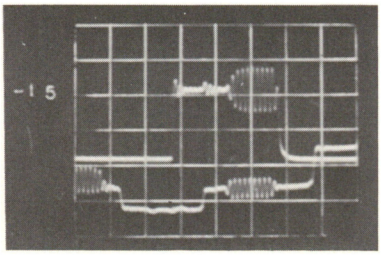


L. Top: Q34 emitter, 5v/cm.
Bottom: ATC Video (P1-20), 1v/cm.

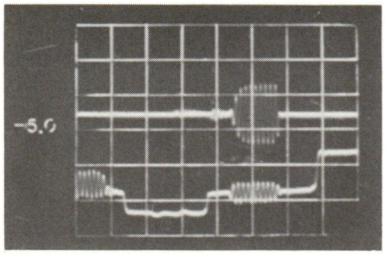
Machine in STOP mode (back-to-back signal). All sweep times 2 μsec/cm unless otherwise noted.

Figure 25—'AND' Multivibrator and Burst Gating Circuits (Continued)

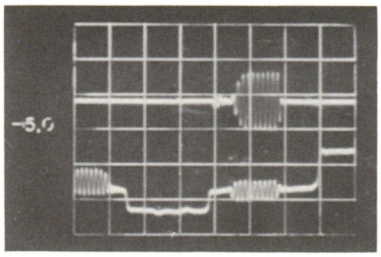




A. Top: Q36 emitter, 2v/cm.
Bottom: ATC Video (P1-20), 0.5v/cm.



B. Top: Q35 base, 1v/cm.
Bottom: ATC Video (P1-20), 0.5v/cm.



C. Top: Q35 emitter, 1v/cm.
Bottom: ATC Video (P1-20), 0.5v/cm.

Machine in STOP mode (back-to-back signal). All sweep times 2 μsec/cm.

Figure 26—Subcarrier Amplifier and Burst Separator Quad

D. Subcarrier Amplifier and Burst Separator Quad

The ATC video signal at the emitter of transistor Q30 in the video input circuit is fed to the series resonant network consisting of resistor R103, capacitor C42, and variable inductor L1 (figure 26). Variable inductor L1 is tuned so that the series network is resonant at the 3.58 mc subcarrier frequency utilized in machines operating on 525-line standards, and thus provides the chroma signal with a low impedance path to amplifier transistor Q37. In the event that inductor L1 becomes de-tuned, or if the machine is to be operated on 625-line standards, the inductor must be re-tuned as instructed below under *Adjustments*.

The signal current passed by the series tuned circuit is shunted to a-c ground by chroma clamp transistor Q38 during the non-burst interval, thereby providing rejection of the undesired portion of the chroma signal in addition to the rejection which is provided by quad Z1 as explained below. Transistor Q38 and associated circuit components form a box car circuit, and the transistor is normally biased into saturation by current withdrawn from its base. When transistor Q38 is saturated it shunts the d-c current flowing through resistor R102, as well as the signal current, and thereby holds amplifier transistor Q37 in cut-off. The positive-going (delayed) edge of the output pulse from delay multivibrator Q22-Q23 drives the base potential of transistor Q38 positive with respect to the emitter potential, due to the action of capacitor C45, thus driving Q38 into cut-off (figure 26A). As capacitor C45 discharges through resistor R107 the base potential of transistor Q38 falls toward −20 volts, and when the base potential becomes slightly more negative than −10 volts the transistor is biased into saturation once again. Thus transistor Q38 remains cut off for approximately 7 microseconds, as determined by the rate at which capacitor C45 discharges through resistor R107.

During the cut-off interval of transistor Q38 a bias current flowing through resistor R102 allows common-base amplifier transistor Q37 to conduct and

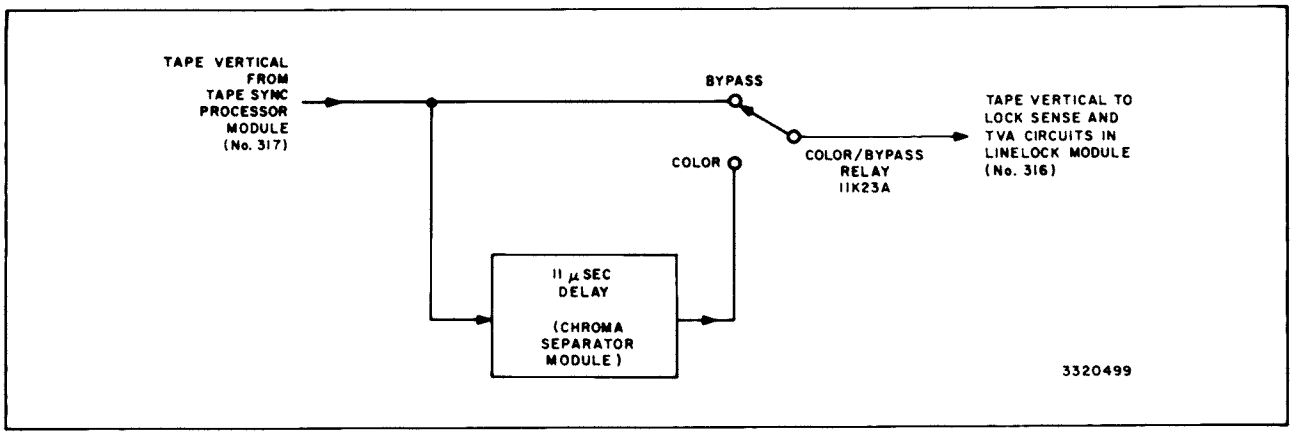


Figure 27—Tape Vertical Signal Path

thereby amplify the signal current from the series tuned circuit. The collector potential of transistor Q37 is −20 volts when the transistor is cut off (during the non-burst interval), and rises to its normal operating potential of −15 volts when the transistor is conducting (during the burst interval). Thus the amplified burst signal is superimposed upon a 5 volt step.

The amplified signal at the collector of transistor Q37 is fed directly to the base of emitter follower transistor Q36. Transistor Q36, biased into conduction by current withdrawn from its base, provides the current required to drive quad Z1 and isolates the quad from the preceding tuned amplifier circuit. Capacitor C41 and resistor R99 form a differentiating network which removes the step from the tuned amplifier output signal and leaves only the edges of the step plus the amplified burst signal to be fed to the quad (figure 26B).

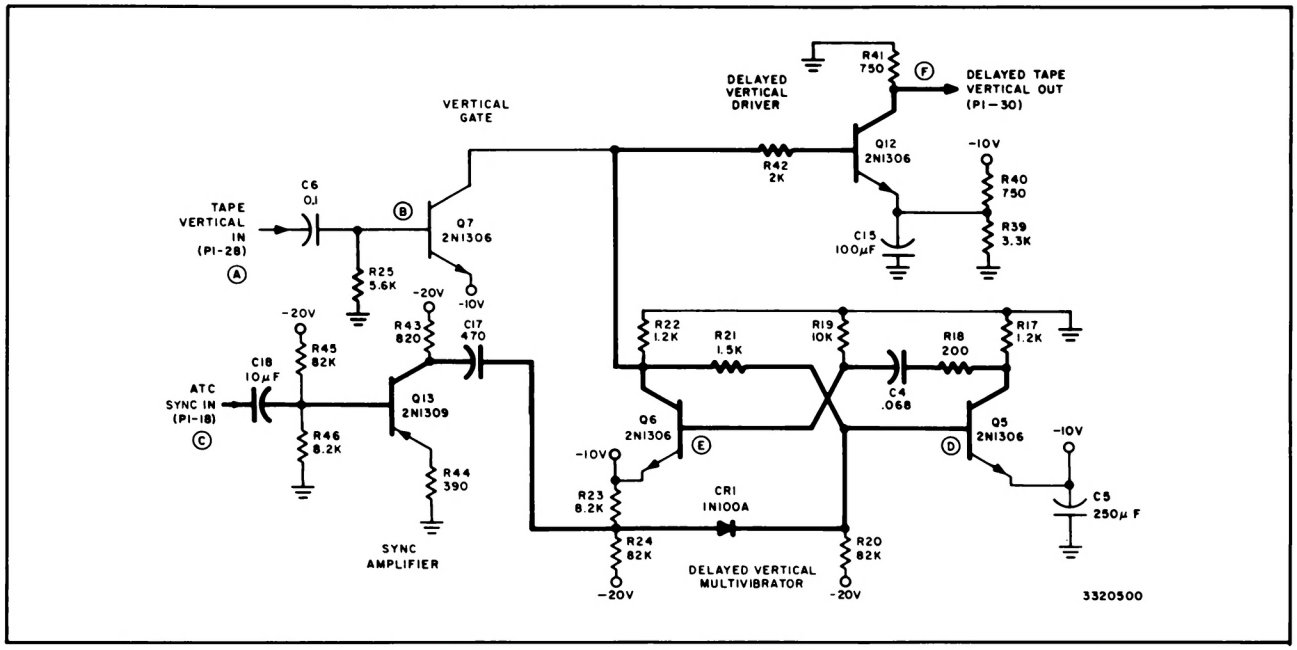
Quad Z1 is controlled by the rough burst gating pulses from the emitter and collector of burst gate transistor Q34. During the interval between gating pulses, the diodes of the quad are reverse-biased and the quad is cut off. Any signal appearing at the emitter of transistor Q36 during this interval will thus be prevented from passing to emitter follower transistor Q35. When the positive- and negative-going gating pulses are simultaneously applied to the quad, the quad diodes are forward biased and the burst signal at the emitter of transistor Q36 is coupled to the base of transistor Q35.

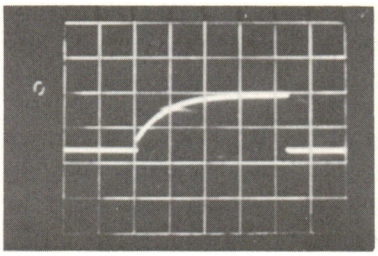
The positive- and negative-going gating pulses fed to quad Z1 overlap by approximately 9 volts, as mentioned above in the discussion of burst gate transistor Q34, and this potential appears across resistors R96 and R97 in series with the quad. Thus the current flowing through the quad when the gating pulses appear is determined by the voltage developed due to overlapping of the gating pulses and the values of resistors R96 and R97. These parameters are such that the current flowing through the quad is approximately 7.3 milliamperes. This current exceeds the amplitude of the burst signal current by a sufficient amount to insure that the quad cannot be cut off by normal burst signal current variations during the gating pulse interval.

The base potential of emitter follower transistor Q35 is established at approximately −5 volts by the divider network consisting of resistors R94 and R95. This potential biases transistor Q35 into conduction and insures that clipping or saturation will not occur when a normal burst signal is applied to its base (figure 26C). The emitter follower action of transistor Q35 provides the current required to drive the output circuit, and the burst signal appearing at the emitter of Q35 (figure 26D) is fed via pin 21 of plug P1 to the burst sensor circuit in the color sensor module (no. 323/C11) and to the burst logic circuit in the color error detector module (no. 326/C14).

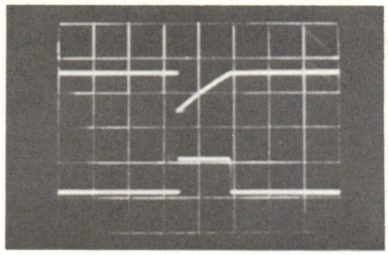
Tape Vertical Delay

The tape vertical signal, generated in the tape sync processor module (no. 317/B20), is fed simultaneously to the BYPASS (normally closed) contact of COLOR/BYPASS relay K23A and to the tape vertical delay circuit in the chroma separator module. (See figure 27.) When the machine is operating in any mode other than normal color ATC or non-phased color (NPC), COLOR/BYPASS relay K23 is deenergized and the tape vertical signal is fed directly to the linelock module. When the machine is operating in the normal color ATC or NPC mode, the COLOR/BYPASS relay is energized and the tape vertical signal then passes through the delay circuit in the chroma separator module before being fed to the linelock module.

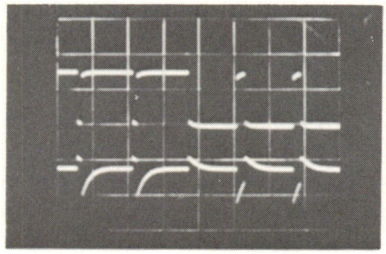




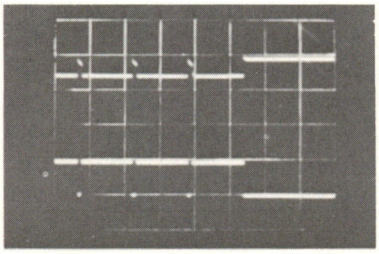
A. Tape Vertical (P1-28), 5v/cm. (2 msec/cm)



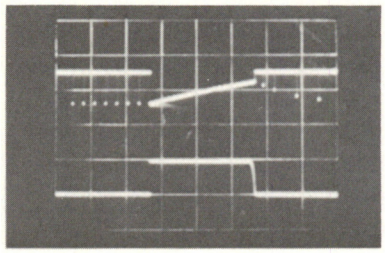
B. Top: Q7 base, 5v/cm. Bottom: Q7 collector, 5v/cm. (200 μsec/cm)



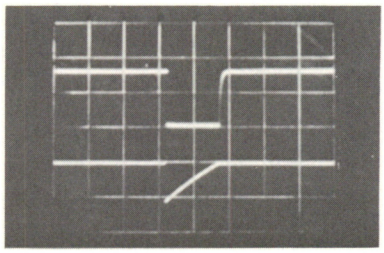
C. Top: ATC Sync (P1-18), 2v/cm. Bottom: CR1 anode, 5v/cm. (20 μsec/cm)



D. Top: Q5 base, 1v/cm. Bottom: Q5 collector, 10v/cm. (20 μsec/cm)



E. Top: Q6 base, 10v/cm. Bottom: Q6, Q7 collector, 5v/cm. (100 μsec/cm)



F. Top: Q12 collector, 5v/cm. Bottom: Q7 base, 5v/cm. (200 μsec/cm)

Machine in STOP mode (back-to-back signal).

Figure 28—Tape Vertical Delay

The function of the tape vertical delay circuit is to develop a tape vertical signal which is delayed with respect to the tape vertical signal from the tape sync processor module by an amount equivalent to the total delay inserted into the tape video path by the various delay circuits in the color ATC system. The purpose of the delay (approximately 11 microseconds) is to insure that the signals derived from the tape vertical signal in the lock sense and TVA circuits of the pixlock servo system will be well within the "lock-in" range required for proper operation of these circuits. Waveforms shown with the schematic diagram (figure 28) and the timing diagram (figure 29) will aid in clarifying the following circuit explanation.

The tape vertical signal from the tape sync processor module is a negative-going pulse occurring at a 60-cycle rate (50-cycle rate in machines operating on 625-line standards), as shown in figure 28A, and is fed to the box car circuit of transistor Q7 via pin 28 of plug P1. Vertical gate transistor Q7 is normally biased into saturation by the current withdrawn from its base and, when saturated, the potential at its base and collector is approximately −10 volts. Due to the action of capacitor C6, the negative-going edge of the incoming tape vertical pulse drives the base potential of transistor Q7 to approximately −16 volts and the transistor is cut off. Then, as capacitor C6 discharges through resistor R25 the base potential of transistor Q7 goes toward ground and, when the base potential becomes positive with respect to −10 volts, the transistor is biased into saturation once again (figure 28B). Thus the duration of the cut-off interval of transistor Q7 is determined by the amplitude of the incoming tape vertical signal in conjunction with the rate at which capacitor C6 discharges through resistor R25.

When vertical gate transistor Q7 is cut off its collector potential remains clamped at −10 volts by the collector potential of transistor Q6 in the delayed vertical multivibrator circuit until the multivibrator is triggered into its unstable state, at which time the potential rises to approximately −5 volts. Therefore the collector potential of transistor Q7, and thus the potential at the base of delayed vertical driver transistor Q12, is determined by the state of both transistor Q7 itself and the delayed vertical multivibrator Q5-Q6. Multivibrator Q5-Q6 is in turn controlled by sync separated from the delayed tape video signal, as explained in the paragraphs below.

In the color ATC mode, the signal appearing at pin 18 of plug P1 is composite sync which has been separated from the tape video signal in the ATC reference module (no. 226/B14) of the monochrome ATC system after the video signal has passed through the various delay circuits in the color ATC system. Thus the separated sync signal has been subjected to a total delay of approximately 11 microseconds before reaching the tape vertical delay circuit.

The delayed composite sync signal (figure 28C) is coupled to the base of sync amplifier transistor Q13. Transistor Q13, biased into conduction by a potential of approximately −1.8 volts applied to its base from the divider network consisting of resistors R45 and R46, amplifies and inverts the composite sync signal. The output signal at the collector of transistor Q13 is differentiated to produce a series of positive- and negative-going spikes timed to the leading and trailing edges respectively of the incoming composite sync signal. The positive- and negative-going spikes are then fed to the anode of diode CR1 (figure 28C, bottom). Diode CR1 is biased so that only the positive-going spikes will be passed on to the base of transistor Q5 in the delayed vertical multivibrator circuit.

Transistors Q5-Q6 and associated circuit components form the monostable delayed vertical multivibrator. In the multivibrator stable state transistor Q6 is biased into saturation while transistor Q5 is biased at cut-off. The base potential of transistor Q5 is established by the divider network consisting of resistors R20 and R21 connected between the −20 volt bus and the common collector potential of transistors Q6 and Q7. When either transistor Q6 or vertical gate transistor Q7 is saturated, the common collector potential is −10 volts. The potential applied to the base of transistor Q5 is then approximately −10.2 volts, and this is sufficient to hold Q5 in cut-off until a positive-going spike is fed to its base via diode CR1 from the sync amplifier circuit. The positive-going spikes appearing at the base of transistor Q5 drive Q5 into conduction; however, positive-going spikes which appear at the base of Q5 when gating transistor Q7 is saturated have no effect on the multivibrator action because the collector potential of transistor Q6 is clamped at −10 volts by the collector potential of transistor Q7. Therefore, the first positive-going spike appearing at the base of transistor Q5 after transistor Q7 has been cut off begins the multivibrator timed cycle. Since this positive-going spike corresponds to the leading edge of the second vertical sync pulse separated from the delayed tape video signal (figure 29), multivibrator Q5-Q6 is triggered 11 microseconds after the undelayed tape vertical signal has driven vertical gate transistor Q7 into cut-off.

During the multivibrator stable state (transistor Q6 saturated; transistor Q5 cut off) the base potential of transistor Q6 is approximately −10 volts dc with respect to the collector potential of transistor Q5. When transistor Q5 is triggered into conduction to begin the multivibrator timed cycle (unstable state) its collector potential immediately falls to −10 volts. Since the potential across capacitor C4 cannot change instantaneously, the base potential of transistor Q6 remains −10 volts with respect to the collector potential of transistor Q5 and is thus approximately −20 volts with respect to ground. This potential biases transistor Q6 into cut-off, and Q6 then remains cut off while its base potential rises toward ground as capacitor C4 discharges through resistor R19. When the potential at the base of transistor Q6 becomes slightly positive with respect to its emitter potential, Q6 is biased into saturation once again and the timed cycle ends.

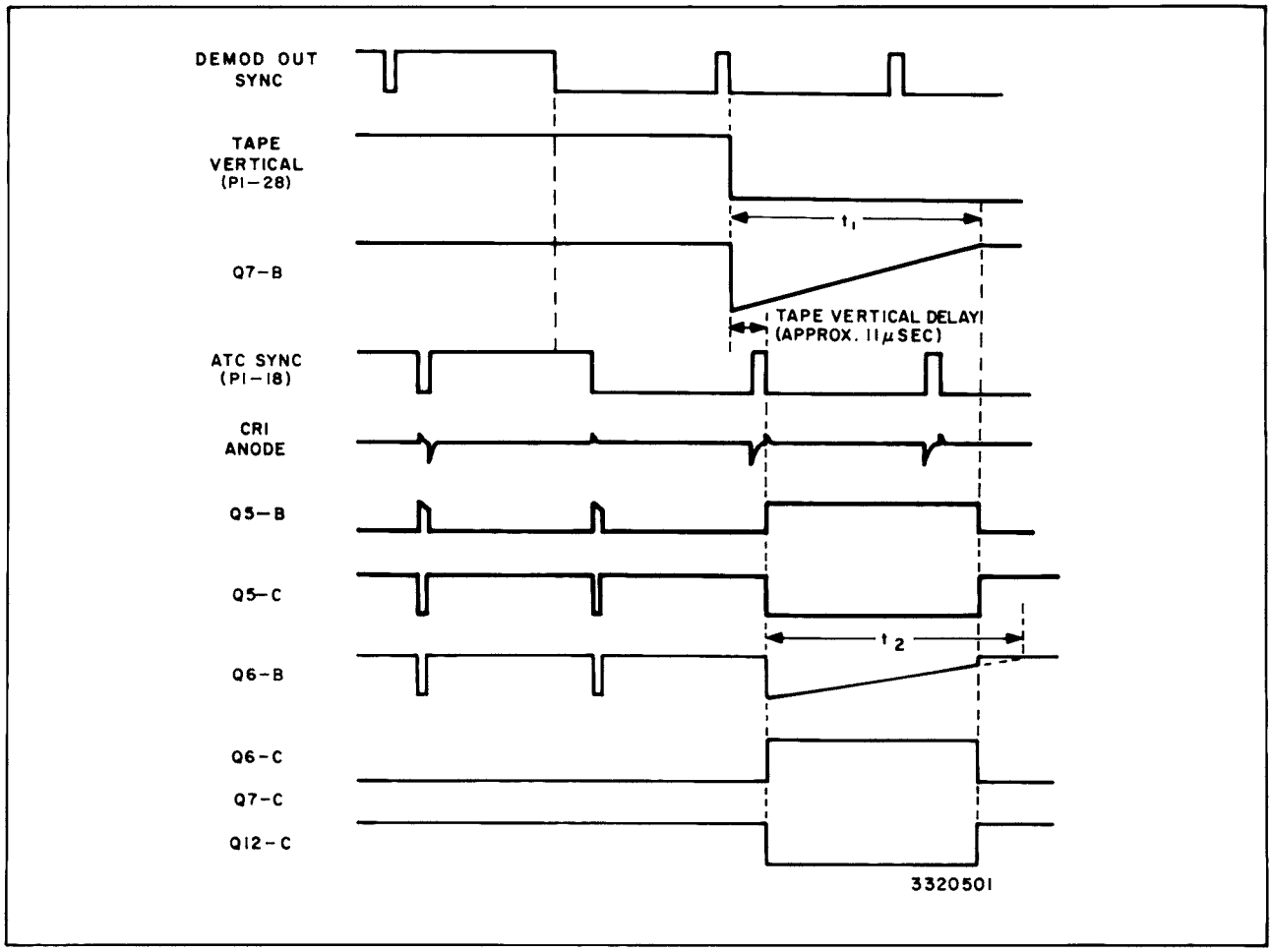


Figure 29—Delayed Tape Vertical Waveform Timing Relationships

The timed cycle of the multivibrator is established by the values of capacitor C4 and resistor R19, and the values chosen are such as to cause the cycle to exceed the "off" period of vertical gate transistor Q7 (as determined by the values of capacitor C6 and resistor R25 in the base circuit of Q7). This arrangement insures that the multivibrator will be triggered only once during the "off" period of transistor Q7 and hence at a vertical rate. The timing diagram (figure 29) indicates the relationship between t_1, the "off" period of transistor Q7, and t_2, the timed cycle of multivibrator Q5-Q6. Note that although t_2 exceeds t_1, the multivibrator timed cycle is actually shortened because of the fact that transistor Q5 is driven into cut-off when Q7 returns to its "on", or saturated, state. In the timing diagram it should also be noted that t_1 and t_2 have been greatly compressed on the time scale so that each entire period may be shown.

When transistor Q5 is saturated (during the multivibrator timed cycle), its base potential is −10 volts. The voltage divider network consisting of resistors R21 and R22 connected between the −10 volt potential at the base of transistor Q5 and ground then establishes the common collector potential of transistors Q6 and Q7 at approximately −5 volts. Therefore the common collector potential of transistors Q6 and Q7 varies between −10 volts when either transistor is saturated and −5 volts when both are cut off, and the positive-going pulse shown in figure 28E (bottom) results.

The positive-going pulse in the common collector circuit of transistors Q6 and Q7 is fed to the base of delayed vertical driver transistor Q12. The divider network consisting of resistors R39 and R40 establishes a bias potential of approximately −8.1 volts dc at the emitter of transistor Q12. Therefore, the positive-going pulse applied to its base drives transistor Q12 into saturation and a negative-going pulse appears in its collector circuit (figure 28F). The negative-going pulse at the collector of transistor Q12 is the delayed tape vertical output signal which is fed through pin 30 of plug P1 to the linelock module via the COLOR contact of COLOR/BYPASS relay K23A.

Adjustments

The following chroma separator module adjustment procedures are part of the system setup adjustments, and once set should not normally require re-adjustment. Test equipment required when making the adjustments consists of a dual-trace oscilloscope such as the *Tektronix Type 535-A* or the equivalent.

Color Output Level

1. Place the chroma separator module on a module extender.

2a. In TR-22 machines rotate the FM standards switch (module no. 205) to COLOR STD 1 or 2 position; in TR-3 machines rotate the demodulator output switch (module no. A18) to COLOR position; in TR-4 machines rotate both the demodulator output switch and the modulator switch (module nos. A18 and A2) to COLOR position.

b. In all machines rotate the selector switch on the ATC delay/output module (no. 223/B11) to COLOR ATC or NON-PHASED COLOR position.

3. In TR-22 and TR-4 machines feed a color bar signal (split field with 100% white bar), 3.58 mc subcarrier (4.43 mc subcarrier to machines operating on 625-line standards), and sync to the machine, and operate the machine in STOP mode (MOD/DEMOD). In TR-3 machines, play back a test tape containing 100% white bar; or, remove the ATC video out pins (nos. 31 and 15) from the demodulator output module receptacle at the rear of the machine and feed a 1 volt peak-to-peak video signal containing white bar information to the pins.

4. Connect one probe of the dual-trace oscilloscope to test point TP1 (SEP IN) of the chroma separator module, and connect the other oscilloscope probe to test point TP2 (LPF OUT).

5. Adjust potentiometer R3 (COLOR OUTPUT LEVEL) so that the white bar amplitude is the same at both test points, as observed on the dual-trace oscilloscope (i.e., so that the low pass filter and amplifier circuits present unity gain).

6. If no further adjustments are to be made, reinsert the module into its receptacle.

High-Pass Balance

1. Follow steps 1, 2, and 3 of the *Color Output Level* adjustment procedure above.

2. Connect one probe of the dual-trace oscilloscope to test point TP3 (CHR OUT).

3. Set up the oscilloscope for a vertical rate presentation, and adjust potentiometer R10 (HI-PASS BALANCE) so that the base-line during the vertical interval is aligned with the base-line during the remainder of the field.

4. If no further adjustments are to be made, reinsert the module into its receptacle.

Gate Delay

1. Follow steps 1, 2, and 3 of the *Color Output Level* adjustment procedure above.

2. Connect one probe of the dual-trace oscilloscope to pin 20 (ATC VID IN) of plug P1, and connect the other probe to the collector of transistor Q24.

3. Set up the oscilloscope for a horizontal rate presentation.

4. Adjust potentiometer R106 (GATE DELAY) so that the delayed (positive-going) edge of the pulse at the collector of transistor Q24 trails the leading (negative-going) edge of ATC sync by 3.6 microseconds.

5. If no further adjustments are to be made, reinsert the module into its receptacle.

Burst Gate Width

1. Follow steps 1, 2, and 3 of the *Color Output Level* adjustment procedure above.

2. Connect one probe of the dual-trace oscilloscope to the emitter of transistor Q34.

3. Adjust potentiometer R84 (BURST GATE WIDTH) for a pulse width of 4.0 microseconds, as observed on the oscilloscope.

4. If no further adjustments are to be made, reinsert the module into its receptacle.

Subcarrier Tuning

NOTE: The subcarrier filter network has been factory tuned for the 3.58 mc subcarrier utilized by machines operating on 525-line standards. If the machine is to be operated on 625-line standards, the filter network must be re-tuned for a 4.43 mc subcarrier.

1. Follow steps 1, 2, and 3 of the *Color Output Level* adjustment procedure above.

2. Connect one probe of the dual-trace oscilloscope to pin 21 (TAPE BURST OUT) of plug P1 and, while observing the oscilloscope, tune inductor L1 for maximum burst amplitude.

3. Re-insert the chroma separator module into its receptacle.

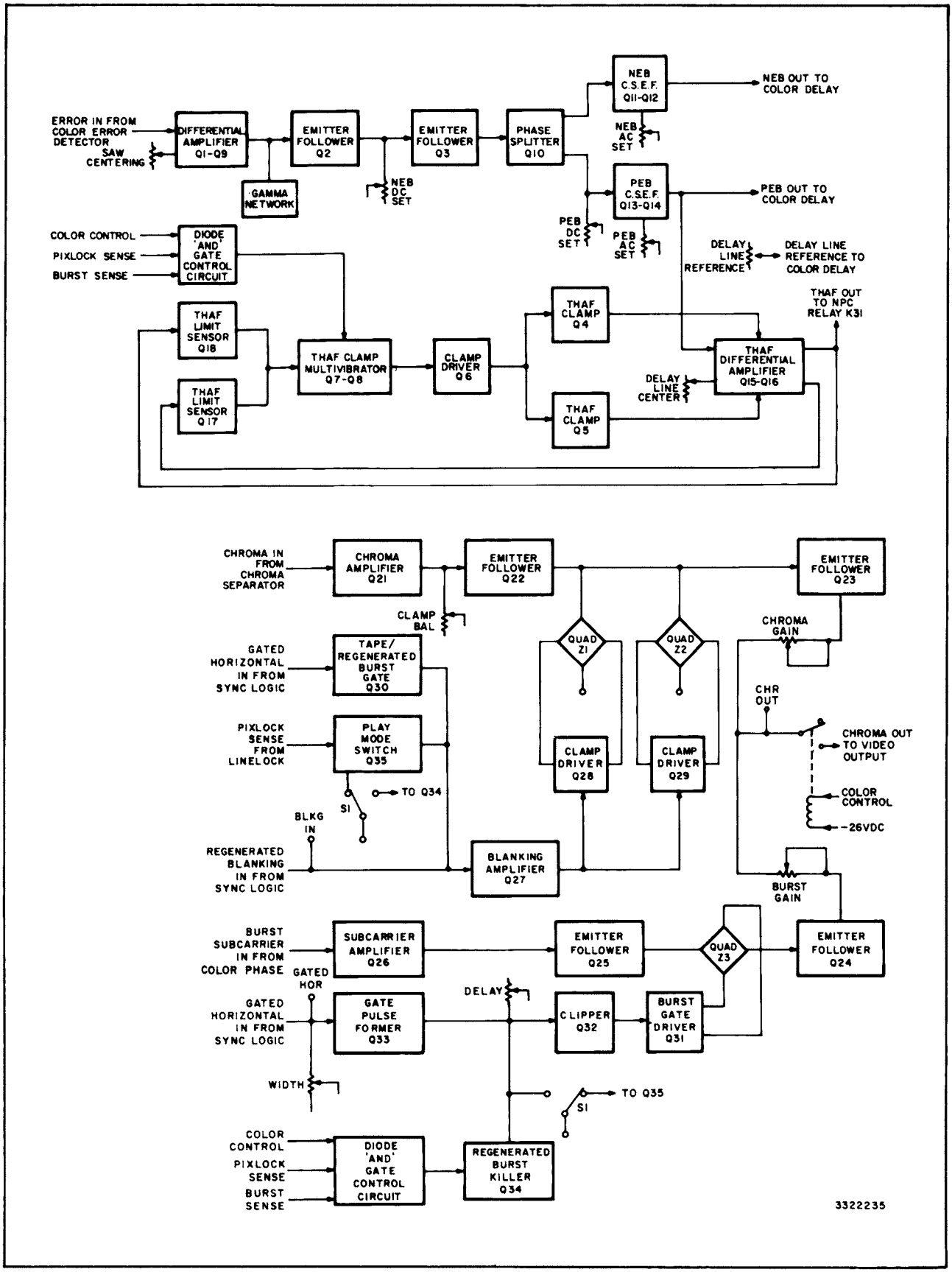


Figure 30—Color Processor Module Block Diagram

COLOR PROCESSOR MODULE (231/C15)

Circuit Description

General

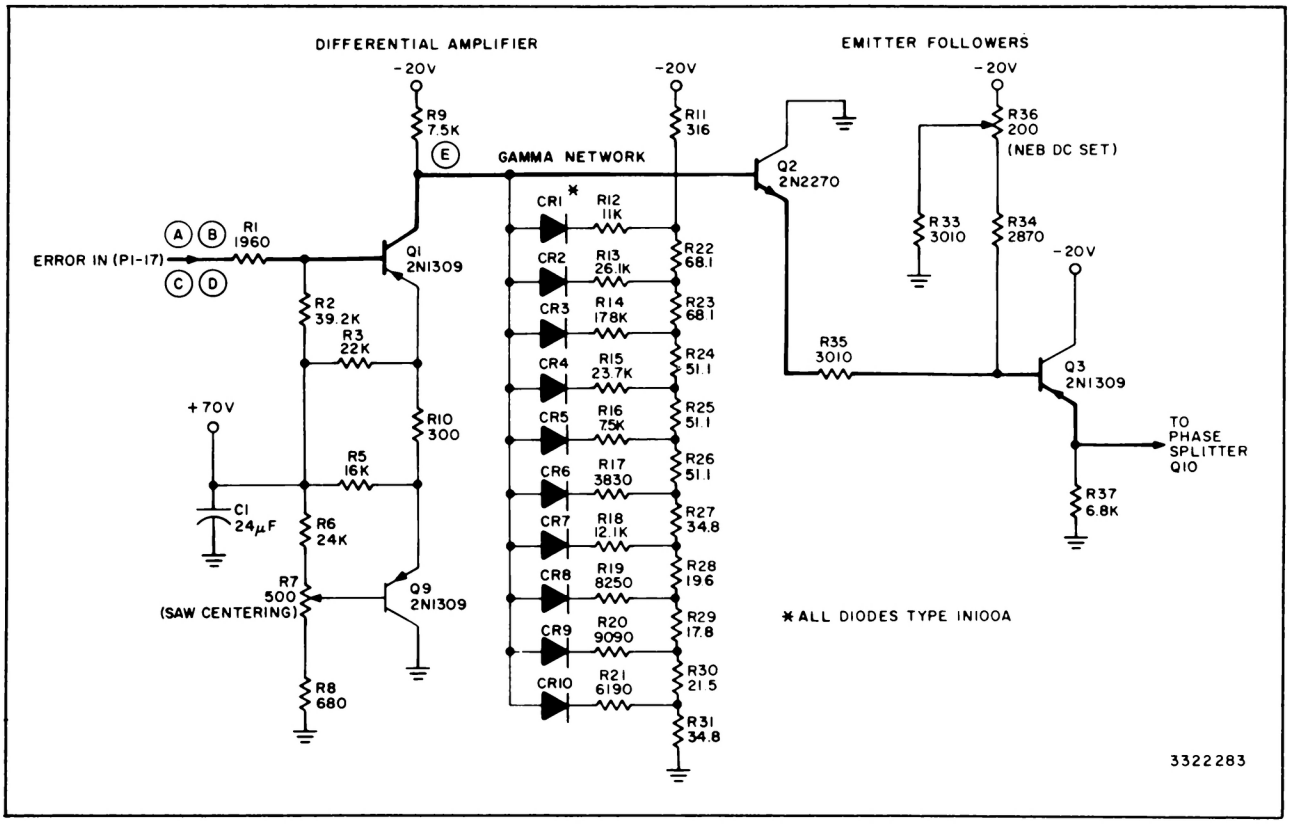
The color processor module (no. 231/C15), shown in block diagram form in figure 30, contains circuits which perform two general functions in the color ATC system. One of the functions is to generate the PEB (positive error bus) and NEB (negative error bus) potentials which are utilized in controlling the delay provided by the electronically variable video delay line in the color delay module. In conjunction with the formation of the PEB potential, circuitry is also provided for the development of the THAF (tape horizontal alignment, fine) error signal utilized in a closed-loop servo which controls the headwheel motor phase in such a manner as to cause the average PEB and NEB potentials to be equal to the voltage equivalent of the center of the video delay line delay range. The other general function performed by color processor module circuitry is to clamp the blanking interval of the chroma signal from the chroma separator module so that regenerated sync and regenerated burst may be inserted, and to produce the regenerated burst by separating a portion of the burst subcarrier signal from the color phase module.

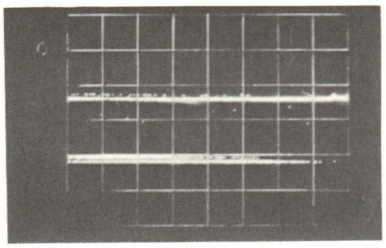
The PEB and NEB potentials are developed from an error signal obtained from the color error detector module. The error signal is an indication of the phase relationship between the reference subcarrier and tape burst signals, and is generated by sampling the slope of a sawtooth waveform derived from the reference subcarrier with a pulse derived from tape burst. The phase error signal varies linearly as the phase difference between reference subcarrier and tape burst fluctuates. However, the characteristics of the video delay line in the color delay module are such that the delay varies non-linearly in response to a linearly varying d-c potential impressed across it. It is desired that the delay of the video delay line vary linearly; therefore it is necessary to convert the linearly varying phase error signal to a non-linear potential having gain characteristics which match the delay characteristics of the video delay line. The non-linear conversion is accomplished by a differential amplifier circuit incorporating a gamma network containing resistors having values calculated to produce a non-linear output which compensates for the non-linearity of the video delay line.

The non-linear error signal is split in phase, and signals of opposite polarity drive complementary symmetry emitter followers which produce the PEB and NEB potentials. It is important that the PEB and NEB potentials be equal and opposite in polarity, with respect to the delay line reference voltage (nominally −10 volts) to which the video signal in the electronically variable video delay line is referred, over the entire phase error signal range; therefore DC SET potentiometers are provided to insure that a change in NEB will be accompanied by an equal and opposite change in PEB. In addition to the DC SET potentiometers, AC SET potentiometers are provided as a means of adjusting the transient behavior of the PEB and NEB potentials so that their rise times will be as nearly equal and opposite as possible in response to a step of error such as occurs at switching when vacuum guide error is present.

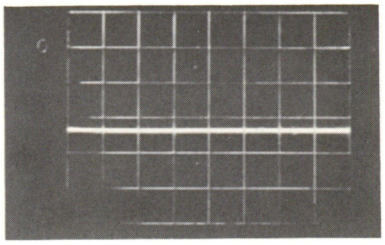
The center of the delay range of the video delay line in the color delay module occurs at a PEB potential of +2.9 volts and a NEB potential of −2.9 volts with respect to the delay line reference potential. Since it is desired that the average PEB and NEB occur at these respective potentials, an error signal is developed which changes the phase of the tape signal in such a direction as to cause the average sampling on the trapezoid waveform slope to produce an error voltage that results in a PEB potential of +2.9 volts with respect to the delay line reference potential. The error signal is designated THAF (tape horizontal alignment, fine), and is derived from a comparison of the PEB potential with a reference voltage, set by means of a potentiometer, in a differential amplifier circuit. The THAF clamping circuit prevents the THAF error signal from exceeding a certain magnitude in either the positive or the negative direction, and thereby minimizes the "cracking effect" (i.e., sampling at alternate extremes of the sawtooth waveform slope). The THAF error signal is developed only during color tape playback in the normal color ATC or non-phased color mode. Under any other conditions a clamping circuit in the color error detector module provides a steady potential which corresponds to zero phase error, thereby maintaining a PEB potential of +2.9 volts with respect to the delay line reference potential and therefore a THAF signal of zero. (Refer to the *Systems* section of this instruction book for a detailed description of the closed THAF loop.)

The chroma signal fed to the color processor module consists of the high frequency components which have been separated from the color video signal in the chroma separator module. In the color processor module the chroma signal is clamped during specific intervals according to the operating conditions of the machine, so that regenerated portions of the signal may be inserted later. When the machine is playing back a color tape while "locked" in the pixlock (or

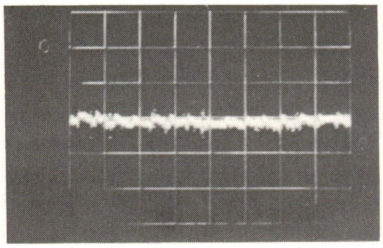




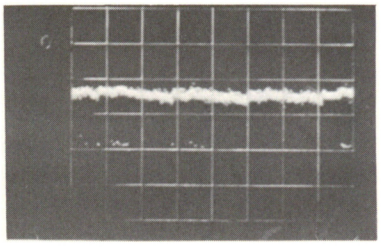
A. Error In (P1-17), 0.5v/cm. STOP mode—cracking.



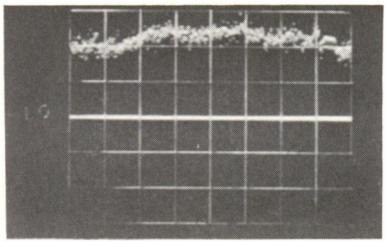
B. Error In (P1-17), 0.5v/cm. STOP mode—cracking clamped.



C. Error In (P1-17), 0.5v/cm.



D. Error In (P1-17), 0.5v/cm. SAW CENTERING misadjusted.



E. Top: Q1 collector, 2v/cm. Bottom: Delay line reference (DLR).

Playback in COLOR ATC mode unless otherwise noted. All sweep times 2 msec/cm.

Figure 31—Non-Linear Amplifier

linelock) servo mode the entire blanking interval is clamped, thus allowing the insertion of regenerated burst and regenerated sync. When the machine is operating in the STOP (MOD-DEMOD) mode, or is playing back a color tape in a non-pixlock (or linelock) servo mode, only the sync interval is clamped and the chroma output signal contains original burst. Clamping is accomplished by cascaded diode quads controlled by pulses triggered from the leading edge of blanking and having widths which are determined by the operating conditions of the machine.

Regenerated burst is obtained by separating a portion of the burst subcarrier signal fed to the color processor module from the color phase module. Separation is accomplished by utilizing a diode bridge (quad) controlled by gating pulses timed to gated horizontal from the sync logic module. The gating pulses insure that the proper number of cycles of burst are separated and that separation is timed so that regenerated burst will occur at precisely the correct moment to obtain a breezeway interval of 0.5 microsecond. During color tape playback in the normal color ATC or non-phased color mode with the machine "locked" in the pixlock (or linelock) servo mode, regenerated burst is inserted into the back porch interval of the signal from the chroma separator module and therefore the chroma signal fed to the video output module contains regenerated burst. If for any reason the machine fails to achieve a "lock" in the pixlock (or linelock) servo mode, a burst killer circuit disables the regenerated burst generator and the chroma clamp interval is shortened so that the chroma signal fed to the video output module contains original burst. A momentary contact pushbutton switch is provided which may be utilized in disabling the regenerated burst generator and shortening the chroma clamp interval at any time in the event that it is desired to obtain a chroma output signal containing original burst.

Phase Error Non-Linear Amplifier

The purpose of the non-linear amplifier circuit, shown in figure 31, is to provide non-linear amplification of the error signal derived from the phase comparison of tape burst and the reference subcarrier signal in the color error detector module (no. 326/C14). The output from the non-linear amplifier circuit is converted into the PEB (positive error bus) and NEB (negative error bus) potentials which control the delay of the non-linear electronically variable delay line in the color delay module (no. 324/C12). The non-linear amplifier circuit includes a differential amplifier and a gamma network containing resistors having values calculated to produce a non-linear output which compensates for the non-linearity of the video delay line. A potentiometer (SAW CENTERING) in the differential amplifier circuit is utilized in varying the operating conditions of the circuit which in turn cause the THAF (tape horizontal alignment, fine) error signal to vary so that in the development of the incoming phase error signal, sampling will occur higher or lower on the sawtooth waveform slope. This enables average sampling to be centered on the sawtooth waveform slope, thus providing a maximum sampling range and therefore minimizing the possibility of incurring the "cracking effect". (Refer to the *General* circuit discussion at the beginning of the module circuit description for a brief explanation of the THAF closed loop servo.)

The phase error signal generated in the color error detector module is fed to the base of amplifier transistor Q1 via pin 17 of plug P1 and resistor R1. The degree of conduction of transistor Q1 is determined by the level of the incoming error signal, and the operating point of the transistor is established by voltage reference transistor Q9. Assuming zero phase error, the potential at pin 17 of plug P1 is approximately −1.2 volts and transistor Q1 is biased into conduction by current withdrawn from its base by the potential at the junction of resistors R1 and R2. Simultaneously, transistor Q9 is biased into conduction by current withdrawn from its base by the potential at the center-arm of potentiometer R7 (SAW CENTERING). As the incoming phase error signal goes positive with respect to the zero error level the conduction of transistor Q1 decreases, thereby allowing current to flow through resistor R10 and increase the conduction of transistor Q9. Conversely, as the error signal goes negative the conduction of transistor Q1 increases as additional current is supplied to its emitter via resistor R10, and the conduction of transistor Q9 decreases correspondingly.

When the THAF feedback loop to the headwheel servo is closed (i.e., the machine is playing back a color tape normally), the average potential at the collector of transistor Q1 is established at a certain value which satisfies the conditions of the loop. This value is determined by the current flowing through transistor Q1, which in turn is equal to the sum of the currents flowing through resistors R3 and R10. The current flowing through resistor R10 depends upon the average potentials appearing at the bases of transistors Q1 and Q9. Therefore, if the potential at the base of transistor Q9 is changed by varying potentiometer R7 (SAW CENTERING), the current

flowing through resistor R10, and thus the potential at the collector of transistor Q1, will attempt to follow this change. This action will cause the THAF loop to adjust the headwheel phase in such a direction that the average error signal fed to the base of transistor Q1 will change to maintain the collector potential of Q1 at that value which satisfies the conditions of the loop. The THAF loop responds only to average error signal changes; therefore, instantaneous error signal changes on a line-by-line basis will cause corresponding changes in the current flowing through transistor Q1.

Typical error signals fed to pin 17 of plug P1 during various machine operating conditions are shown in A, B, C, and D of figure 31. Figure 31A shows the error signal when the machine is operating in the STOP mode with the error clamp potential removed and the "cracking effect" artificially simulated, while figure 31B shows the error signal when the machine is operating normally in the STOP mode with the error signal clamped at the level which corresponds to zero phase error. Figure 31C shows the error signal input during normal color tape playback, while figure 31D shows the error signal when the SAW CENTERING potentiometer (R7) is misadjusted and some "cracking" occurs.

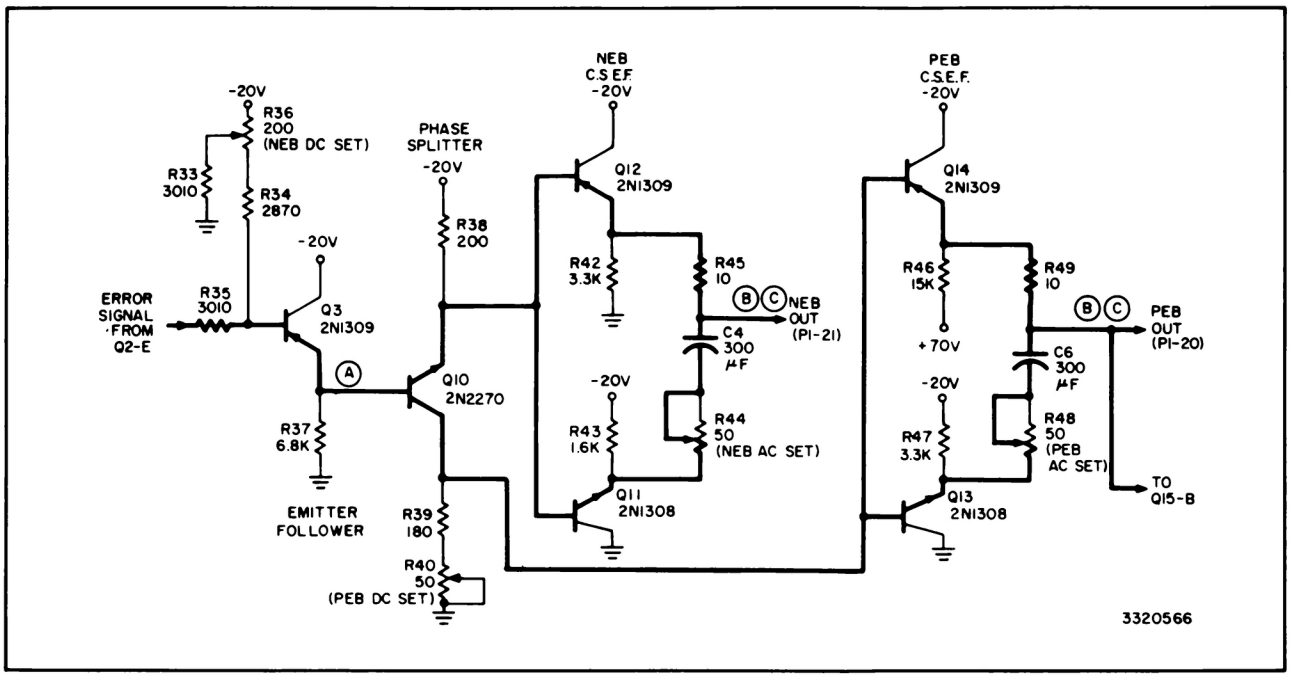
> NOTE: The error clamp potential may be removed when the machine is operating in the STOP mode by grounding the pixlock sense bus at pin 12 of plug P1. The "cracking effect" may be created when the clamping potential is removed by varying the SYSTEM PHASE control on the color phase module front panel until "cracking" occurs.

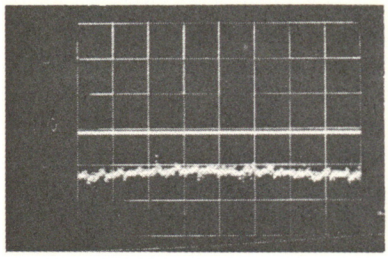
When the phase error is zero, the collector potential of transistor Q1 is maintained at a level which results in a PEB potential of +2.9 volts with respect to the delay line reference potential by the THAF error signal. As the phase error signal varies from its zero error level the signal variations are amplified non-linearly by the action of a gamma network which is connected in parallel with load resistor R9 in the collector circuit of transistor Q1. (Refer to figure 31.) The gamma network consists of ten diode-resistor sections which, taken as a whole, function as a single resistor whose resistance varies non-linearly in accordance with the signal appearing at the collector of transistor Q1. Since this "resistor" is in parallel with resistor R9 the load impedance of transistor Q1, and thus the gain, varies non-linearly.

The potential appearing at the collector of transistor Q1, established by comparison of the phase error signal with the reference voltage, also appears at the anodes of diodes CR1 through CR10 in the gamma network. When this potential is positive with respect to the negative potential applied to the cathode of a particular diode, that diode is forward-biased and its associated resistors are inserted into the circuit in parallel with resistor R9. The cathode potential of each diode is established by the voltage divider network consisting of resistor R11 and resistors R22 through R31 connected between the −20 volt bus and ground. When the phase error is zero the collector potential of transistor Q1, as determined by the THAF error signal, is approximately −5 volts and diodes CR1 through CR5 are forward-biased while the remaining diodes are cut off. The total resistance inserted into the collector circuit of transistor Q1 by the gamma network remains constant as long as the phase error is zero. As the phase error signal varies in the positive direction a greater number of diodes will become forward-biased and the total number of resistors added in parallel will increase, thus decreasing the total load resistance. Conversely, as the phase error signal varies in the negative direction fewer diodes will be forward-biased and the total number of resistors added in parallel will decrease, thus increasing the total load resistance.

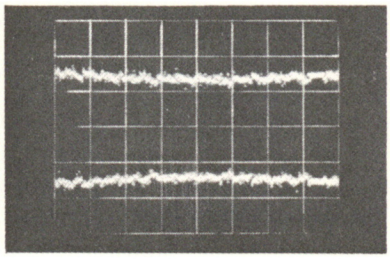
Therefore, during normal color tape playback the linear fluctuations of the phase error signal are amplified non-linearly by the differential amplifier in conjunction with the gamma network. The characteristics of the non-linear amplifier are such that its gain may be represented by a series of straight line segments, having varying slopes, which approximate a curve, and the values of the resistors in the gamma network have been chosen to obtain a curve which compensates for the non-linear delay curve of the video delay line.

The fluctuating error signal appearing at the collector of transistor Q1 (figure 31E) is fed directly to the base of emitter follower transistor Q2. Transistor Q2 isolates the non-linear amplifier from the succeeding circuitry, and the fluctuating error signal appearing at its emitter is fed to the base of emitter follower transistor Q3 via resistor R35. Transistor Q3 further isolates the non-linear amplifier circuit and provides the current required to drive phase splitter transistor Q10. Potentiometer R36 (NEB DC SET) is utilized in adjusting the bias potential at the base of transistor Q3. Since transistor Q3 functions as an emitter follower and its emitter is connected directly to the base of phase splitter transistor Q10, the setting of potentiometer R36 also determines the biasing potential at the base of Q10 as explained below in the *PEB and NEB Potential Development* discussion.

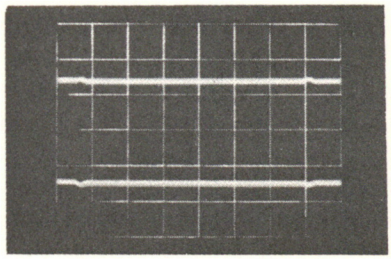




A. Top: Delay line reference (DLR).
Bottom: Q3 emitter, 2v/cm.
(2 msec/cm)



B. Top: PEB (P1-20), 2v/cm.
Bottom: NEB (P1-21), 2v/cm.
(2 msec/cm)



C. Top: PEB (P1-20), 2v/cm.
Bottom: NEB (P1-21), 2v/cm.
(10 μsec/cm)

Playback in COLOR ATC mode.

Figure 32—PEB and NEB C.S.E.F. Circuits

Development of PEB and NEB Potentials

The PEB (positive error bus) and NEB (negative error bus) potentials control the electronically variable video delay line in the color delay module. Proper operation of the delay line requires that the PEB and NEB potentials be equal and opposite in polarity with respect to the delay line reference potential to which the video signal is referred, and that the rise times of PEB and NEB be as nearly equal as possible in response to a "step" of error such as occurs at switching when guide error is present. To meet these requirements the phase splitter and complementary symmetry emitter followers in the PEB and NEB potential development circuits are controlled by four potentiometers, as shown in figure 32. The NEB DC SET potentiometer is a bias adjustment which is utilized in setting the operating point of the phase splitter and consequently shifts both the PEB and NEB potentials when adjusted. The PEB

DC SET potentiometer is the phase splitter gain adjustment, affecting the PEB potential only, and is set so that a change in the error signal fed to the phase splitter results in opposite polarity output signals of equal amplitude. In addition, the complementary symmetry emitter followers contain the PEB AC SET and NEB AC SET potentiometers. These potentiometers are utilized in obtaining an a-c balance between the PEB and NEB potentials; i.e., in adjusting the transient behavior of PEB and NEB in response to a step of error.

The non-linear error signal appearing at the emitter of transistor Q2 is fed to the base of emitter follower transistor Q3. Potentiometer R36 and resistors R34 and R35 form a divider network between the −20 volt supply and the collector potential of transistor Q1 (gamma voltage) which establishes the d-c potential at the base of transistor Q3. The resistance values of these components are such that the d-c level at the base of transistor Q3 will insure final PEB and NEB potentials which fall within the operating voltage range of the electronically variable video delay line (±1 to 8 volts with respect to the delay line reference potential). The base potential of transistor Q3 may be varied over a narrow range by adjusting potentiometer R36, and Q3 is biased into conduction by current withdrawn from its base by the negative potential at the junction of resistors R34 and R35. Transistor Q3 provides isolation and the current required to drive phase splitter transistor Q10, and the error signal appearing at its emitter (shown during color tape playback in figure 32A) is fed directly to the base of Q10. Since potentiometer R36 controls the bias potential at the base of transistor Q3 (over a narrow range), it also controls the d-c potential at the emitter of Q3 and thus at the base of transistor Q10. Therefore, potentiometer R36 (NEB DC SET) is utilized in setting the operating point of transistor Q10.

Phase splitter transistor Q10 is biased into conduction by current flowing into its base from the potential at the emitter of transistor Q3, and error signals of opposite polarity appear at its emitter and collector. Potentiometer R40 (PEB DC SET) in the collector circuit of transistor Q10 functions as a gain adjustment and is provided as a means of matching the collector impedance with that of the emitter of Q10 (including the loads imposed by the transistors which follow). This insures that a change in potential at the emitter of transistor Q10, due to a change in the error signal applied to its base, will be accompanied by an equal and opposite change in potential at its collector.

The error signal appearing at the emitter of phase splitter transistor Q10 is fed simultaneously to the bases of complementary symmetry emitter follower transistors Q11-Q12. Similarly, the signal appearing at the collector of transistor Q10, 180 degrees out of phase with that at the emitter, is fed simultaneously to the bases of complementary symmetry emitter follower transistors Q13-Q14. Transistor Q12 conducts when a comparatively slowly varying error signal appears at the emitter of transistor Q10, and also responds to a rapid negative-going change, or "step", in the error signal. However, due to the high capacitance load in the color delay module, transistor Q12, a PNP type, cannot respond with sufficient rapidity to a positive-going step in error. Therefore it is the function of transistor Q11, an NPN type, to provide a rapid response to the positive-going step, or transient. Capacitor C4 (300 microfarads) in the emitter circuit of transistor Q11 passes the varying, or a-c, component of the error signal appearing at the emitter of Q11 and blocks the d-c component. The error signal passed by capacitor C4 is added to the error signal at the emitter of transistor Q12, and the combined signal is fed via pin 21 of plug P1 to the color delay module as the NEB control voltage (figures 32B and 32C, bottom).

Complementary symmetry emitter follower transistors Q13-Q14 function in exactly the same manner as transistors Q11-Q12, and the combined error signal appearing at the junction of capacitor C6 and resistor R49 is fed via pin 20 of plug P1 to the color delay module as the PEB control voltage (figures 32B and 32C, top). The PEB error signal is also fed to transistor Q15 in the differential amplifier circuit described below in the THAF error signal development discussion.

Potentiometers R44 and R48 are utilized in altering the transient behavior of transistors Q11 and Q13 respectively to insure that the rise times of the PEB and NEB error signals are as nearly equal as possible. In obtaining the proper a-c balance between the PEB and NEB error signals, potentiometer R44 (NEB AC SET) is adjusted to match the impedance of resistor R49 so that the response of transistors Q11 and Q14 will be identical for a positive-going step in error signal appearing at the base of phase splitter transistor Q10. Similarly, potentiometer R48 (PEB AC SET) is adjusted to match the impedance of resistor R45 so that the response of transistors Q13 and Q12 will be identical for a negative-going step in error signal appearing at the base of transistor Q10. (Refer to the *Adjustment* section at the end of the module circuit description.)

THAF Error Signal Generator and Clamping Circuit

The THAF (tape horizontal alignment, fine) error signal generator produces the THAF error signal which is utilized in maintaining a constant phase relationship between the local reference subcarrier signal and the burst signal appearing on a color tape during playback in the normal color ATC or non-phased color (NPC) mode. The THAF error signal controls a closed-loop servo circuit which varies the head-wheel motor phase to compensate for any change in relative phase between the tape burst and reference subcarrier signals. The operation of the THAF loop itself is explained in detail in the *Systems* section of this instruction book.

As shown in figure 33, the THAF error signal is developed by a differential amplifier circuit wherein the fluctuating PEB potential is compared with a fixed reference voltage. The reference voltage may be manually set by means of a potentiometer, and its value is nominally −7.1 volts (i.e., that potential which corresponds to the center of the delay range of the video delay line in the color delay module). During normal color tape playback, when the PEB potential is equal to the delay line centering voltage the THAF error signal is zero (ground). As the PEB potential fluctuates about the zero error level in response to shifting phase relationships between the tape burst and reference subcarrier signals, the THAF error signal also varies. However, due to the action of the THAF clamping circuit the THAF error signal variation is limited to approximately ±2 volts. During any machine conditions other than normal color tape playback, the THAF clamping circuit maintains a zero THAF error signal. Thus a THAF error signal appears only during color tape playback in the normal color ATC or non-phased color mode, with the machine "locked" in the pix-lock (or linelock) servo mode.

A. THAF Differential Amplifier

Transistors Q15-Q16 and associated circuit components comprise the THAF differential amplifier circuit (figure 33). The signal fed to the base of transistor Q15 is the PEB potential obtained from complementary symmetry emitter follower transistors Q13-Q14 and developed as explained above in the *Development of PEB and NEB Potentials* discussion. The operating point of the differential amplifier is established by potentiometer R64 (DELAY LINE CENTER) in the divider network which also includes resistors R60 and R65. Potentiometer R64 is adjusted to obtain an average PEB potential during tape playback of +2.9 volts with respect to the delay line reference potential which is nominally −10 volts, and the potential appearing at the base of transistor Q16 from the center-arm of the potentiometer is approximately −7.1 volts. Therefore, when the PEB potential applied to the base of transistor Q15 is +2.9 volts with respect to the delay line reference potential, transistors Q15 and Q16 are biased into conduction and currents of equal magnitude flow through the transistors. The component values in the differential amplifier circuit are such that when potentiometer R64 is correctly set a PEB potential of +2.9 volts with respect to the delay line reference potential will result in zero (ground) potential at the collectors of transistors Q15 and Q16. The potential appearing at the collector of transistor Q15 is the THAF error signal; thus when the PEB potential is +2.9 volts with respect to the delay line reference potential the THAF signal is zero.

During color tape playback the phase error signal fluctuates about the zero error level, thereby causing the PEB potential at the base of transistor Q15 to correspondingly vary positive or negative with respect to the nominal value of −7.1 volts. When the PEB potential goes positive with respect to −7.1 volts the emitter current of transistor Q15 increases and, since the current flowing through common emitter resistor R59 remains constant, the emitter current of transistor Q16 decreases accordingly. As mentioned in the above paragraph, a zero phase error results in zero (ground) potential at the collectors of transistors Q15 and Q16, and thus a zero THAF signal. Therefore, as the current flowing through transistor Q15 increases and the current flowing through transistor Q16 decreases, the collector potential of Q15 goes negative with respect to ground and the collector potential of Q16 goes positive. Conversely, when the PEB potential goes negative with respect to the nominal −7.1 volt potential, the differential amplifier operating conditions are reversed and the collector potential of transistor Q15 goes positive with respect to ground while the collector potential of transistor Q16 goes negative. Thus the THAF error signal appearing at the collector of transistor Q15 goes negative when the PEB potential goes positive and vice versa.

It should be noted that the operation of transistor Q15 discussed in the above paragraph pertains to changes in *average* PEB potential. Line-by-line changes will cause the current in transistor Q15 to increase or decrease; however, due to the fact that the large capacitance in the base circuit of Q15 acts as a short circuit to the −10 volt power supply for rapidly changing currents, over a short term period the collector potential of Q15 (THAF error signal)

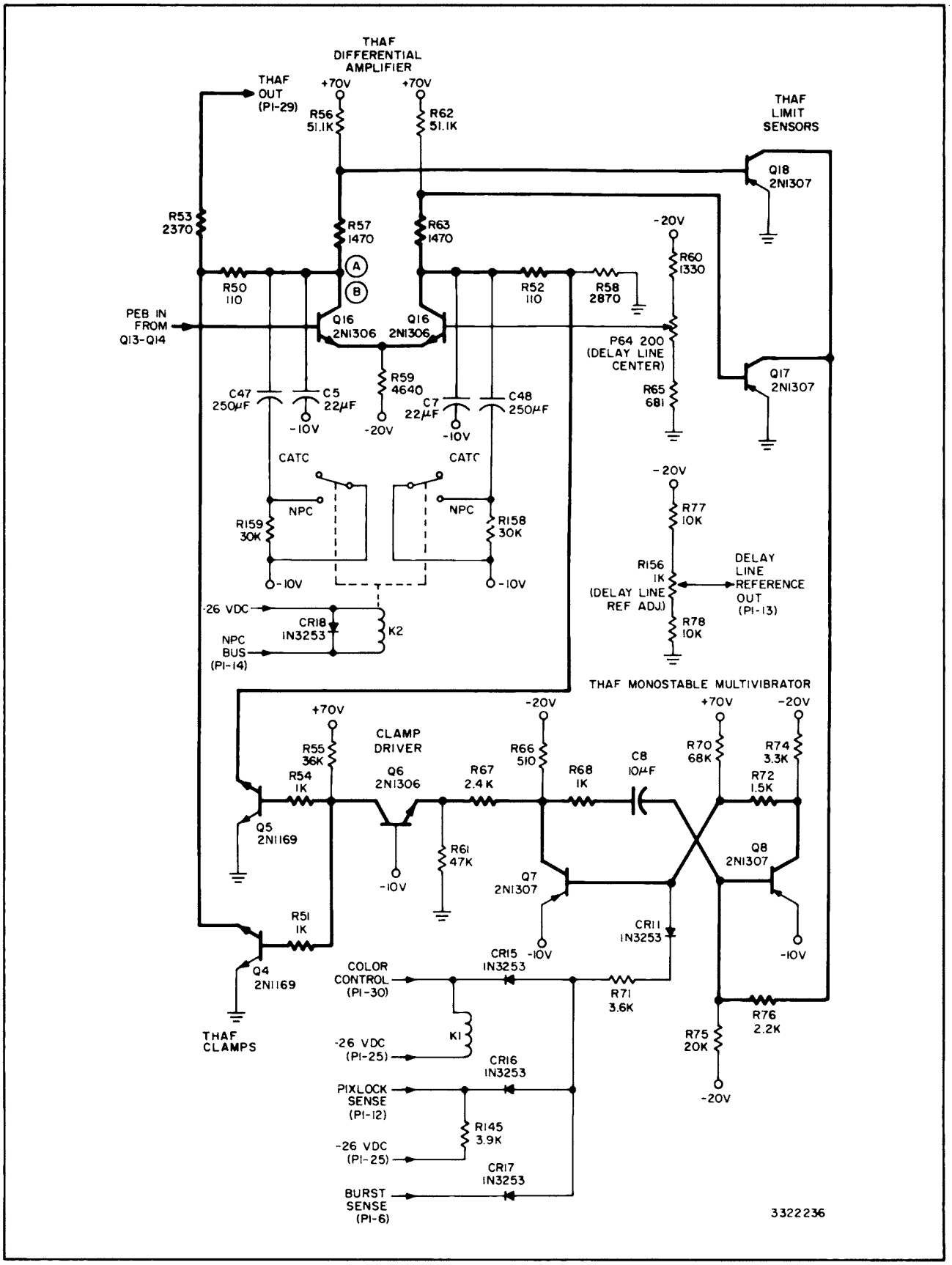
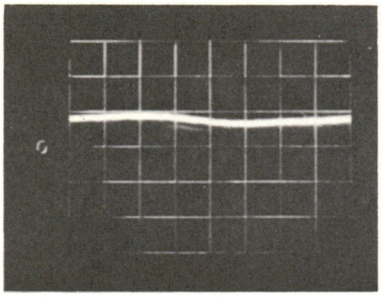
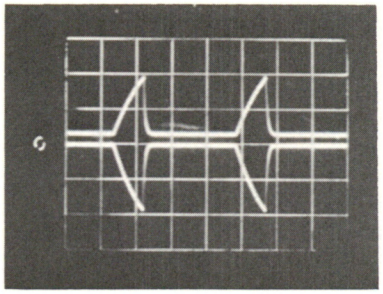


Figure 33—THAF Error Signal Generator and Clamping Circuits



A. Q15 collector, 1v/cm.
PLAY mode.
(2 msec/cm)



B. Top: Q15 collector, 1v/cm.
Bottom: Q16 collector, 1v/cm.
STOP mode (unclamped).
(50 msec/cm)

Figure 33—THAF Error Signal Generator and Clamping Circuits (Continued)

will remain steady. Therefore, only long term (very low frequency) changes will cause the THAF potential to change.

When the average PEB potential goes sufficiently positive to cause a current to flow through transistor Q15 which results in a voltage drop across resistor R57 of approximately 2 volts, the potential at the junction of resistors R56 and R57 is slightly negative with respect to ground and the THAF clamping circuit is activated. Similarly, the THAF clamping circuit is activated when the PEB potential goes sufficiently negative to cause a current to flow through transistor Q16 which results in a voltage drop across resistor R63 of approximately 2 volts and therefore a potential at the junction of resistors R62 and R63 which is slightly negative with respect to ground. The operation of the clamping circuit is described below in the *THAF Clamping Circuit* discussion, and it is sufficient to state here that whenever the THAF error signal attempts to exceed ±2 volts during color tape playback the differential amplifier circuit is clamped and the error signal is returned to zero. Therefore, due to the clamping circuit the THAF error signal appearing at the collector of transistor Q15 varies between the approximate limits of ±2 volts as the PEB potential fluctuates in response to the phase error signal.

If a tape burst signal is not present for any reason, or the machine has failed to "lock-up" in the pixlock servo mode, the 'AND' gate consisting of diodes CR15, CR16, and CR17 controls the THAF multivibrator so that the THAF clamp transistors Q4 and Q5 are saturated and the THAF error signal is thereby clamped at zero.

The THAF error signal is fed via resistors R50 and R53 and pin 29 of plug P1 to NPC relay K31. When the machine is playing back a color tape in the normal color ATC mode, relay K31 is deenergized and the THAF signal is fed to a differential amplifier circuit in the monochrome ATC error detector module (no. 225/B13). During color tape playback in the non-phased color mode, relay K31 is energized and the THAF signal is fed to the color sensor module where it is utilized in modulating the delay developed by a multivibrator, as explained in the color sensor module circuit description. Figure 33A shows the normal THAF error signal appearing at the collector of transistor Q15 when the machine is properly playing back a color tape. Figure 33B shows the signals appearing at the collectors of transistors Q15 and Q16 during machine operation in the STOP mode with the clamp circuit in the color error detector module and the THAF clamp circuit disabled so that an error signal of sufficient amplitude may be introduced which will cause the THAF clamping circuit to function. (Both clamping circuits may be disabled by grounding the common anode connection of 'AND' gate diodes CR15, CR16, and CR17.)

The THAF closed-loop bandwidth and stability are determined by the combined transfer functions throughout the loop. The major time constant in the loop consists of resistor R53 and capacitor C5 when playing back a color tape in the normal color ATC mode and resistor R53 and capacitors C5 and C47 in parallel when playing back a color tape in the non-phased color mode. The closed-loop bandwidth is greater when operating the machine in the non-phased color mode than when operating in the normal color ATC mode, even though the time constant is larger, due to the fact that the open-loop gain is much higher. The time constant in the collector circuit of transistor Q15 is balanced by an equal time constant in the collector circuit of transistor Q16 so that the voltage drive to the THAF limit sensor transistors Q17 and Q18 is equally limited in bandwidth for positive- and negative-going errors. The time constants are switched by relay K2, which is deenergized when operating the machine in the normal color ATC mode and energized when operating in the non-phased color mode and the NPC bus is at ground potential.

B. THAF Clamping Circuit

In the THAF clamping circuit (shown in figure 33) the potential at the junction of resistors R56 and R57 in the collector circuit of differential amplifier transistor Q15 is fed directly to the base of THAF limit sensor transistor Q18, while the potential at the junction of resistors R62 and R63 in the collector circuit of transistor Q16 is fed directly to the base of THAF limit sensor transistor Q17. Transistors Q17 and Q18 are normally biased into cut-off; however, when the PEB potential applied to the base of transistor Q15 varies sufficiently positive or negative to cause the potential at the junction of resistors R56 and R57 or at the junction of resistors R62 and R63 to go slightly negative with respect to ground, Q18 or Q17 will be biased into saturation by current withdrawn from its respective base. Since the collectors of transistors Q17 and Q18 are common, whenever either transistor is saturated the common collector potential is ground. Therefore, at the instant transistor Q17 or transistor Q18 is biased into saturation, resistor R76 in the base circuit of THAF multivibrator transistor Q8 is returned to ground potential.

Transistors Q7-Q8 and associated circuit components comprise the monostable THAF multivibrator. In the multivibrator stable state transistor Q8 is biased into saturation by current withdrawn from its base by the −20 volt supply via resistor R75, and a potential of approximately −10 volts appears at its base and collector. Simultaneously, transistor Q7 is biased into cut-off by a potential of approximately −8 volts applied to its base from the divider network consisting of resistors R70 and R72 connected between the +70 volt supply and the collector potential of transistor Q8, and its collector potential is established at approximately −18 volts by the voltage drop across resistor R66 due to current supplied by common base amplifier transistor Q6 plus current flowing from ground via resistor R61. Thus during the multivibrator stable state the base of transistor Q8 is approximately 8 volts positive with respect to the collector of transistor Q7, and capacitor C8 is charged to this potential difference.

When resistor R76 in the base circuit of transistor Q8 is returned to ground potential due to the saturation of THAF limit sensor transistor Q17 or Q18, current flows from ground to the −20 volt supply via resistors R75 and R76. This action cuts off transistor Q8 and begins the multivibrator timed cycle. At the instant transistor Q8 is cut off, transistor Q7 is biased into saturation by current withdrawn from its base by the −20 volt supply via resistors R72 and R74. When transistor Q7 is biased into saturation its collector potential immediately rises to approximately −10 volts. However, since the potential across capacitor C8 cannot change instantaneously, the base of transistor Q8 remains approximately 8 volts positive with respect to the collector of transistor Q7 and Q8 is held in its cut-off state. Transistor Q8 remains cut off as capacitor C8 charges toward −20 volts via resistor R75 until C8 has charged to a potential which is slightly negative with respect to −10 volts. At this point transistor Q8 is biased into saturation once again by current withdrawn from its base and the multivibrator timed cycle ends. The values of the components in the multivibrator timing circuit are such that the multivibrator timed cycle is approximately 150 milliseconds. When the multivibrator has returned to its stable state it will remain in this state until the next phase error signal excursion occurs which results in a PEB potential that exceeds the established value required to bias either of the THAF limit sensor transistors into saturation.

During normal color tape playback the pixlock sense, burst sense, and color control busses are at ground potential. Diode CR11 is then reverse-biased and multivibrator Q7-Q8 functions as described above. When the ATC function selector switch on

the monochrome ATC delay/output module front panel is in ATC OFF or COLOR OFF position, pin 30 of plug P1 is connected to an open circuit and −26 volts dc is applied to the cathode of diode CR15 from the coil of relay K1 which is utilized in the color processor section of the module. If for any reason the machine has failed to achieve a "lock" in the pixlock (or linelock) servo mode, pin 12 of plug P1 is connected to an open circuit and −26 volts dc is applied to the cathode of diode CR16 via pin 25 of plug P1 and resistor R145. If the tape burst signal is lost for any reason while the machine is otherwise playing back a color tape normally, a burst sense potential of approximately −23 volts dc is applied to the cathode of diode CR17 via pin 6 of plug P1. Therefore, when any of the above three conditions exists, a negative potential appears at the common anode connection of diodes CR15, CR16, and CR17, and diode CR11 is forward-biased. Transistor Q7 is then biased into saturation by current withdrawn from its base by the negative potential via diode CR11 and resistor R71. Transistor Q7 will remain saturated as long as any of the above conditions exist which result in a negative potential at the common anode connection of diodes CR15, CR16, and CR17.

When multivibrator Q7-Q8 is in its stable state, transistor Q7 is cut off and common base amplifier transistor Q6 is biased into conduction by current flowing into its base from the −10 volt supply. The current flowing through transistor Q6 when Q6 is conducting is supplied by the +70 volt supply via resistor R55 and causes a negative potential to appear at the collector of Q6. The negative potential is of sufficient amplitude to hold THAF clamping transistors Q4 and Q5 in cut-off and the THAF clamping circuit therefore has no effect on the operation of differential amplifier transistors Q15-Q16.

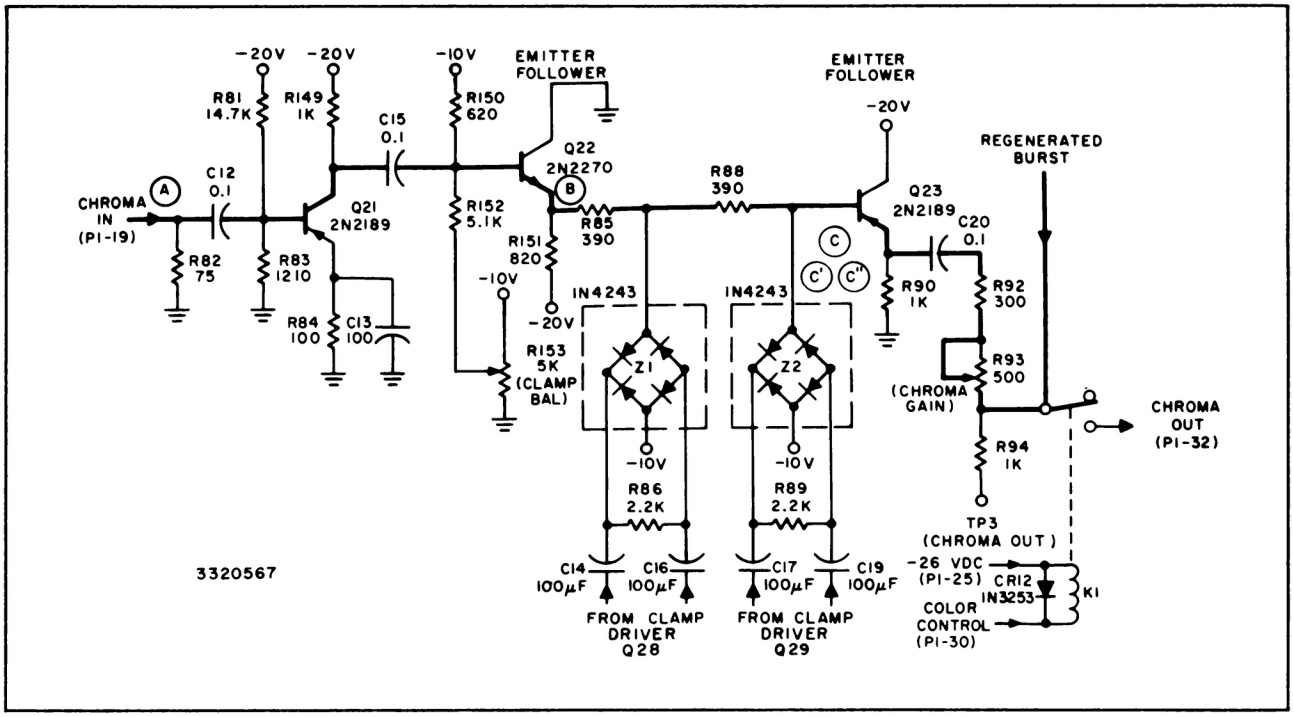
During the multivibrator unstable state transistor Q7 is saturated and the potential at its collector is −10 volts. A potential of approximately −9.5 volts then appears at the emitter of common base amplifier transistor Q6 from the junction of resistors R67 and R61, and Q6 is biased into cut-off. This allows the THAF clamping transistors Q4 and Q5 to be biased into conduction by current supplied to their bases from the +70 volt supply via resistor R55 and resistors R51 and R54.

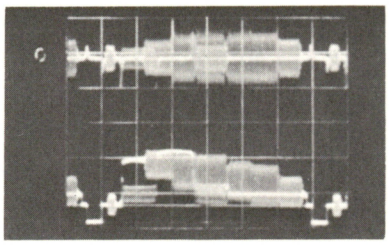
Transistors Q4 and Q5 are bilateral types; i.e., either electrode may function as emitter or collector. As mentioned above, when the PEB potential goes positive with respect to the nominal zero error level of −7.1 volts the potential at the collector of differential amplifier transistor Q15 goes negative with respect to ground and the potential at the collector of transistor Q16 goes positive. In this case, during the clamping interval the upper electrode of transistor Q4 (in figure 33) functions as the emitter and the lower electrode as the collector, and the upper electrode of transistor Q5 functions as the collector and the lower electrode as the emitter. Conversely, as the PEB potential goes negative with respect to the nominal −7.1 volt level the potential at the collector of transistor Q15 goes positive with respect to ground and the potential at the collector of transistor Q16 goes negative, and the functions of the electrodes of transistors Q4 and Q5 are reversed. In either case, however, clamping transistors Q4 and Q5 are saturated; thus the collectors of differential amplifier transistors Q15-Q16 are clamped at ground potential and the THAF error signal is zero.

Chroma Amplifier

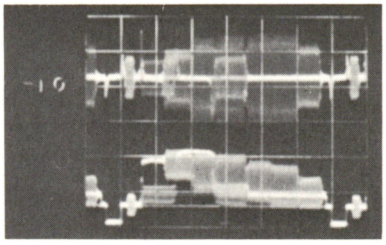
The chroma amplifier circuit (shown in figure 34) amplifies the high frequency components (chroma) that have been separated from the color video signal in the chroma separator module (no. 325/C13). Following amplification, the chroma signal is clamped at approximately −10 volts over specific intervals which are determined by the operating conditions of the machine. During color tape playback with the machine "locked" in the pixlock (or linelock) servo mode the entire blanking interval is clamped. This allows the insertion of regenerated burst, obtained from the burst separator circuit in this module, and the insertion of regenerated sync, developed in the sync logic module (no. 230/B21) and added to the chroma signal in the video output module (no. 233/A22). When the machine is operating in the STOP (MOD-DEMOD) mode, or is playing back a tape in a non-pixlock (or linelock) servo mode, the clamped interval is only from the leading edge of blanking to the trailing edge of sync. In this case the sync interval is clamped to allow the insertion of regenerated sync, as during playback in the pixlock (or linelock) servo mode, however the back porch interval containing the original burst signal is passed along with the remaining chroma information to the chroma output at color control relay K1.

The chroma signal, containing original burst, is fed to the module at pin 19 of plug P1 (figure 34A) and is coupled to the base of transistor Q21 via capacitor C12. Transistor Q21, biased into conduction by

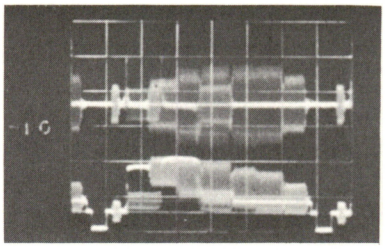




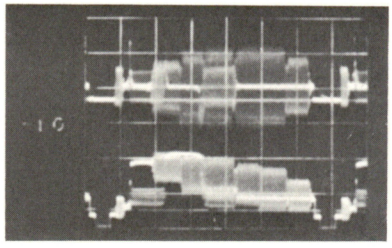
A. Top: Chroma (P1-19), 0.5v/cm.
Bottom: Video out (233), 1v/cm.



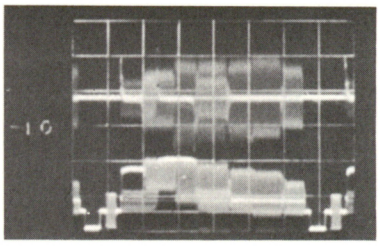
B. Top: Q22 emitter, 1v/cm.
Bottom: Video out (233), 1v/cm.



C. Top: Q23 emitter, 1v/cm.
Bottom: Video out (233), 1v/cm.



C'. Top: Q23 emitter, 1v/cm.
Bottom: Video out (233), 1v/cm.
CLAMP BAL misadjusted.



C". Top: Q23 emitter, 1v/cm.
Bottom: Video out (233), 1v/cm.
PLAY mode.

Machine in STOP mode (back-to-back signal) unless otherwise noted. All sweep times 10 μsec/cm.

Figure 34—Chroma Amplifier

a potential of approximately −2 volts applied to its base from the divider network consisting of resistors R81 and R83, amplifies the chroma signal. Capacitor C13 in the emitter circuit of transistor Q21 provides a slight amount of peaking, and the amplified signal appearing at the collector of Q21 is coupled to the base of emitter follower transistor Q22.

Transistor Q22, biased into conduction by current flowing into its base from the junction of resistors R150 and R152, provides current gain and isolates the chroma amplifier from the succeeding circuitry. The signal appearing at the emitter of transistor Q22 (figure 34B) is subjected to the cascaded clamping circuit consisting of quads Z1 and Z2 before being fed to the base of emitter follower transistor Q23. The operation of the clamping circuit is explained in detail below in the *Clamping Circuit* discussion, and it is sufficient to state here that the entire blanking interval is clamped at approximately −10 volts dc when the machine is playing back a tape in the pixlock (or linelock) servo mode and that only the interval from the leading edge of blanking to the trailing edge of sync is clamped when the machine is operating in a non-pixlock (or linelock) servo mode.

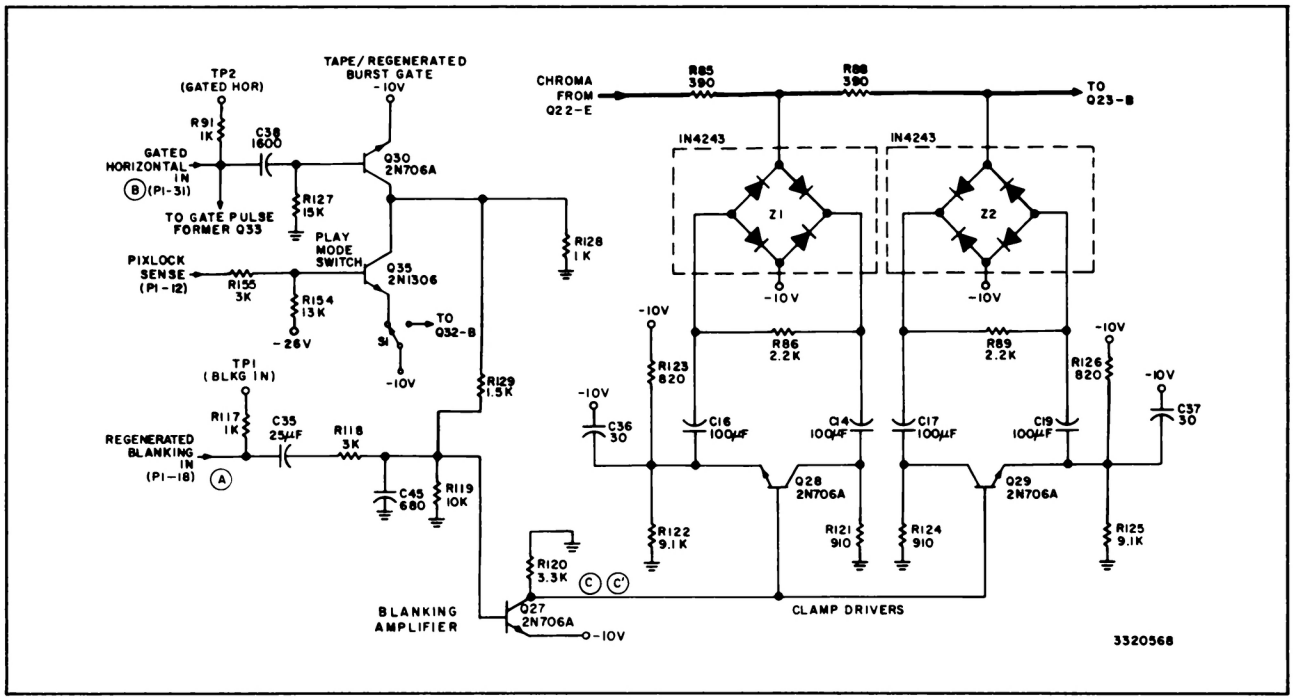
Potentiometer R153 (CLAMP BAL) is utilized in varying the d-c biasing potential at the base of transistor Q22 so that the d-c axis of the signal appearing at the base of transistor Q23 may be made to coincide with the level of the clamping potential provided by quads Z1 and Z2, and thus eliminate the possibility of a "step" during the clamping interval. The range of potentiometer R153 is approximately one volt, and a procedure for properly adjusting the potentiometer is presented under *Adjustments* at the end of the module circuit description.

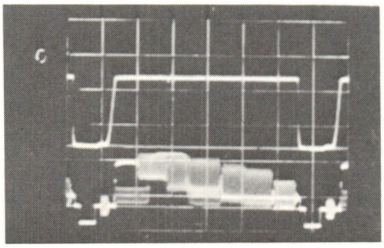
Emitter follower transistor Q23 provides the current required to drive the output circuit and isolates the output from the preceding amplifier and clamping circuits. The signal appearing at the emitter of transistor Q23 during machine operation in the STOP (MOD-DEMOD) mode, with the interval between the leading edge of blanking and the trailing edge of sync clamped, is shown in figures 34C and 34C′. Note in figure 34C′ the "step" appearing on the signal d-c axis due to a misadjustment of CLAMP BAL potentiometer R153. The signal appearing at the emitter of transistor Q23 during tape playback in the pixlock (or linelock) servo mode, with the entire blanking interval clamped, is shown in figure 34C″.

Potentiometer R93 (CHROMA GAIN) is utilized in setting the level of the output signal and is normally adjusted so that the amplitude of the chroma output signal from the color delay module is equal to the amplitude of the signal from the video output module. (A procedure for adjusting potentiometer R93 is provided under *Adjustments* at the end of the circuit description.) Regenerated burst is added to the output signal when the machine is playing back a tape in the pixlock (or linelock) servo mode, and the resulting chroma signal is fed to color control relay K1. If for any reason the machine is not "locked" in the pixlock (or linelock) servo mode, the chroma clamp interval is shortened as mentioned above and the regenerated burst separator circuit is disabled. In this case the chroma output signal fed to relay K1 contains original burst. Momentary contact pushbutton switch S1 is provided for use in the event that it is desired to obtain a chroma output signal containing original burst while the machine is "locked" in the pixlock (or linelock) servo mode. (The operation of switch S1 is described below in the *Chroma Clamping Circuit* discussion.)

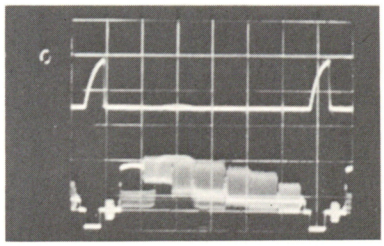
Relay K1, normally deenergized, is energized when the color control bus is at ground potential. The color control bus is at ground potential when all conditions are met for normal machine operation in the color ATC mode. These conditions include the following: (1) the ATC mode switch on the ATC delay/output module (no. 223/B11) must be in COLOR ATC or NON-PHASED COLOR position; (2) in TR-22 machines the FM standards switch (module no. 205) must be in COLOR STD 1 or 2 position or, in TR-3 machines the demodulator output switch (module no. A18) must be in COLOR position or, in TR-4 machines the demodulator output and the modulator switches (module nos. A18 and A2) must both be in COLOR position; and (3) all monochrome and color ATC modules must be securely inserted into their respective receptacles. When the above conditions are met, relay K1 is energized and the chroma signal is fed via pin 32 of plug P1 to the video output module.

Test point TP3 (CHR OUT) is provided for convenience in observing the output chroma signal. It should be noted that due to a very low impedance the level of the signal appearing at test point TP3 will be low. Thus when observing the signal on an oscilloscope it may be necessary to utilize a high gain oscilloscope preamplifier.

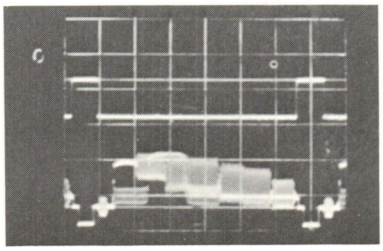




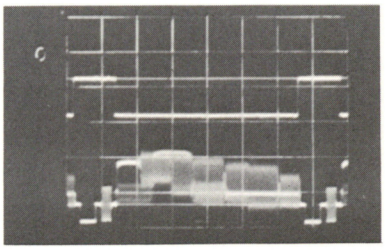
A. Top: Regenerated Blanking (P1-18), 5v/cm. Bottom: Video out (233), 1v/cm.



B. Top: Gated Horizontal (P1-31), 2v/cm. Bottom: Video out (233), 1v/cm.



C. Top: Q27 collector, 5v/cm. Bottom: Video out (233), 1v/cm.



C'. Top: Q27 collector, 5v/cm. Bottom: Video out (233), 1v/cm. PLAY mode.

Machine in STOP mode (back-to-back signal) unless otherwise noted. All sweep times 10 μsec/cm.

Figure 35—Chroma Clamping Circuit

Chroma Clamping Circuit

The purpose of the chroma clamping circuit (figure 35) is to clamp certain portions of the high-pass chroma signal obtained from the chroma separator module, as explained above in the *Chroma Amplifier* circuit discussion. During color tape playback with the machine "locked" in the pixlock (or linelock) servo mode, the entire blanking interval is clamped. When the machine is operated in the STOP (MOD-DEMOD) mode, or is not "locked" in the pixlock (or linelock) servo mode during playback, or momentary contact pushbutton switch S1 is pressed, only the interval between the leading edge of blanking and the trailing edge of sync is clamped. Clamping is accomplished by two diode quads which are cascaded to obtain maximum attenuation. The diode quads are in turn controlled by pulses which are triggered from the leading edge of regenerated blanking and have widths equivalent to either blanking or the interval between the leading edge of blanking and the trailing edge of sync, depending upon the operating conditions of the machine.

The regenerated blanking pulse, fed to the module at pin 18 of plug P1, is obtained from the sync logic module (no. 230/B21) and may be observed at test point TP1 (BLKG IN). The negative-going blanking pulse (figure 35A) is attenuated by the network consisting of resistors R118 and R119, and the attenuated pulse is applied to the base of blanking amplifier transistor Q27. Transistor Q27 is normally biased into saturation by current flowing into its base and the negative-going leading edge of the blanking pulse drives the transistor into cut-off. The duration of the cut-off interval of transistor Q27 is determined by the state of tape regenerated burst gate transistor Q30 in conjunction with the state of play mode switch transistor Q35. These transistors are in turn controlled by the gated horizontal pulse and the operating conditions of the machine respectively.

During tape playback with the machine "locked" in the pixlock servo mode the pixlock sense bus is at ground potential. Ground potential therefore appears at pin 12 of plug P1 and play mode switch transistor Q35 is biased into saturation by current flowing into its base via resistor R155. When transistor Q35 is saturated, the common collector of transistors Q30 and Q35 is at −10 volts. Resistor R129 is then returned to −10 volts and, during the interval between blanking pulses, transistor Q27 is biased into saturation by current flowing into its base via resistor R119. The negative-going leading edge of the regenerated blanking pulse drives transistor Q27 into cut-off, as mentioned above, and, since during playback in the pixlock mode transistor Q35 remains saturated continuously, Q27 remains cut off for the entire blanking interval regardless of the condition of tape regenerated burst gate transistor Q30.

When the machine is in the STOP (MOD-DEMOD) mode, or is not "locked" in the pixlock (or linelock) servo mode during playback, the pixlock sense bus is essentially an open circuit and play mode switch transistor Q35 is biased into cut-off by −26 volts applied to its base via resistor R154. In this case blanking amplifier transistor Q27 is controlled by tape regenerated burst gate transistor Q30 during the blanking interval. Transistor Q30 is normally biased into saturation by current flowing into its base via resistor R127. The input signal fed to transistor Q30 is the gated horizontal pulse which is fed to the module at pin 31 of plug P1 from the sync logic module. The incoming positive-going pulse (figure 35B) is differentiated by the network consisting of capacitor C38 and resistor R127, and the negative-going spike resulting from the differentiation of the trailing edge of the pulse drives transistor Q30 into cut-off. The circuit of transistor Q30 functions as a boxcar circuit; therefore the transistor remains cut off as capacitor C38 discharges toward ground through resistor R127. When capacitor C38 has discharged to a potential which is slightly positive with respect to −10 volts transistor Q30 becomes biased into saturation once again.

During the blanking pulse interval transistor Q27 remains cut off as long as transistor Q30 is saturated and the common collector potential of transistors Q30 and Q35 is −10 volts. However, when transistor Q30 is driven into cut-off by the negative-going trailing edge of the gated horizontal pulse the −10 volt potential is removed from the common collector of transistors Q30 and Q35 and transistor Q27 is biased into saturation once again by current flowing into its base. The R127-C38 time constant of the boxcar circuit of transistor Q30 is sufficiently long to insure that Q30 will remain cut off for the remainder of the blanking interval. Thus under any conditions other than tape playback in the pixlock (or linelock) servo mode, transistor Q27 will be driven into cut-off by the leading edge of the regenerated blanking pulse and will be returned to its saturated state by the trailing edge of the gated horizontal pulse. It should be noted that during tape playback in the pixlock servo mode transistor Q35 may be manually cut off by pressing momentary contact pushbutton switch S1. When switch S1 is pressed transistor Q27 is controlled solely by tape regenerated burst gate transistor Q30, and therefore the cut-off duration of Q27

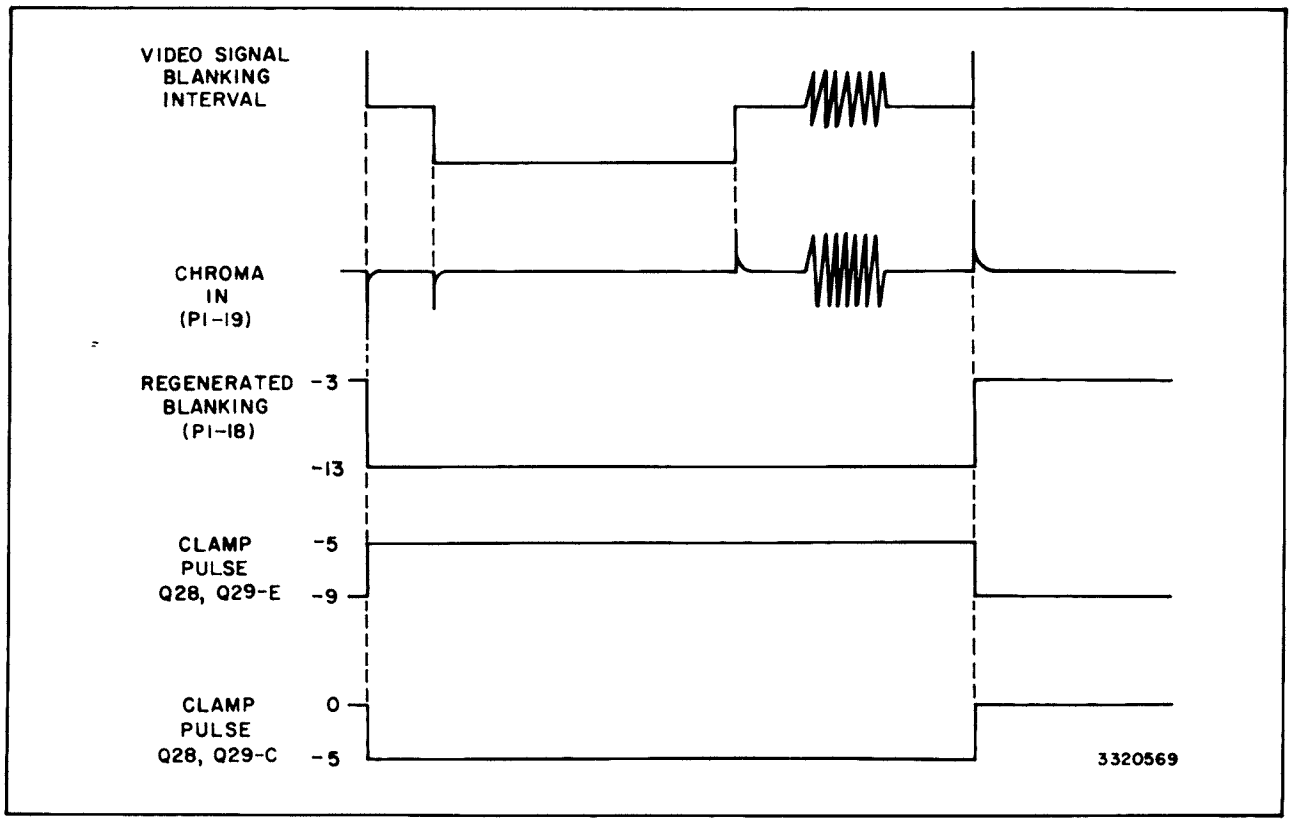


Figure 36—Clamp Pulse Development During Playback in the Pixlock Servo Mode

is from the leading edge of the regenerated blanking pulse to the trailing edge of the gated horizontal pulse; i.e., the effect on transistor Q27 is exactly the same as when the machine is operating in a non-pixlock (or linelock) servo mode.

When blanking amplifier transistor Q27 is saturated its collector potential is −10 volts and this potential appears at the bases of parallel clamp driver transistors Q28 and Q29. The d-c divider networks in the emitter circuits of transistors Q28 and Q29 establish emitter potentials of approximately −9 volts and the transistors are thereby biased into cut-off. At the instant transistor Q27 is driven into cut-off by the leading edge of the regenerated blanking pulse the −10 volt potential is removed from its collector and clamp driver transistors Q28 and Q29 are then biased into conduction by current supplied to their bases via resistor R120. The current drawn through resistor R120 by transistors Q28 and Q29 results in a potential of approximately −4 volts at the collector of transistor Q27 when Q27 is cut off. Thus the signal appearing at the collector of transistor Q27 is a positive-going pulse having a width equivalent to the entire blanking interval during tape playback in the pixlock (or linelock) servo mode and a width equivalent to the interval from the leading edge of blanking to the trailing edge of sync during non-pixlock (or linelock) servo operation (figures 35C and 35C′).

The positive-going pulse appearing at the collector of transistor Q27, and thus at the bases of clamp driver transistors Q28 and Q29, results in the appearance of positive-going pulses at the emitters of Q28 and Q29 and negative-going pulses at the collectors of Q28 and Q29. (See timing diagrams, figures 36 and 37.) The positive- and negative-going clamp pulses are coupled to diode quads Z1 and Z2 via 100 microfarad capacitors, and the polarities of the clamping pulses are such that the quad diodes are forward-biased during the clamping interval. When the quad diodes are forward-biased the junction of resistors R85 and R88 and the junction of resistor R88 and the base of emitter follower transistor Q23 are clamped at −10 volts. Therefore, during normal color tape playback in the pixlock (or linelock) servo mode the entire blanking interval (sync plus burst) of the chroma signal is clamped at approximately −10 volts. However, during non-pixlock operation only the interval from the leading edge of blanking to the trailing edge of sync is clamped at approximately −10 volts.

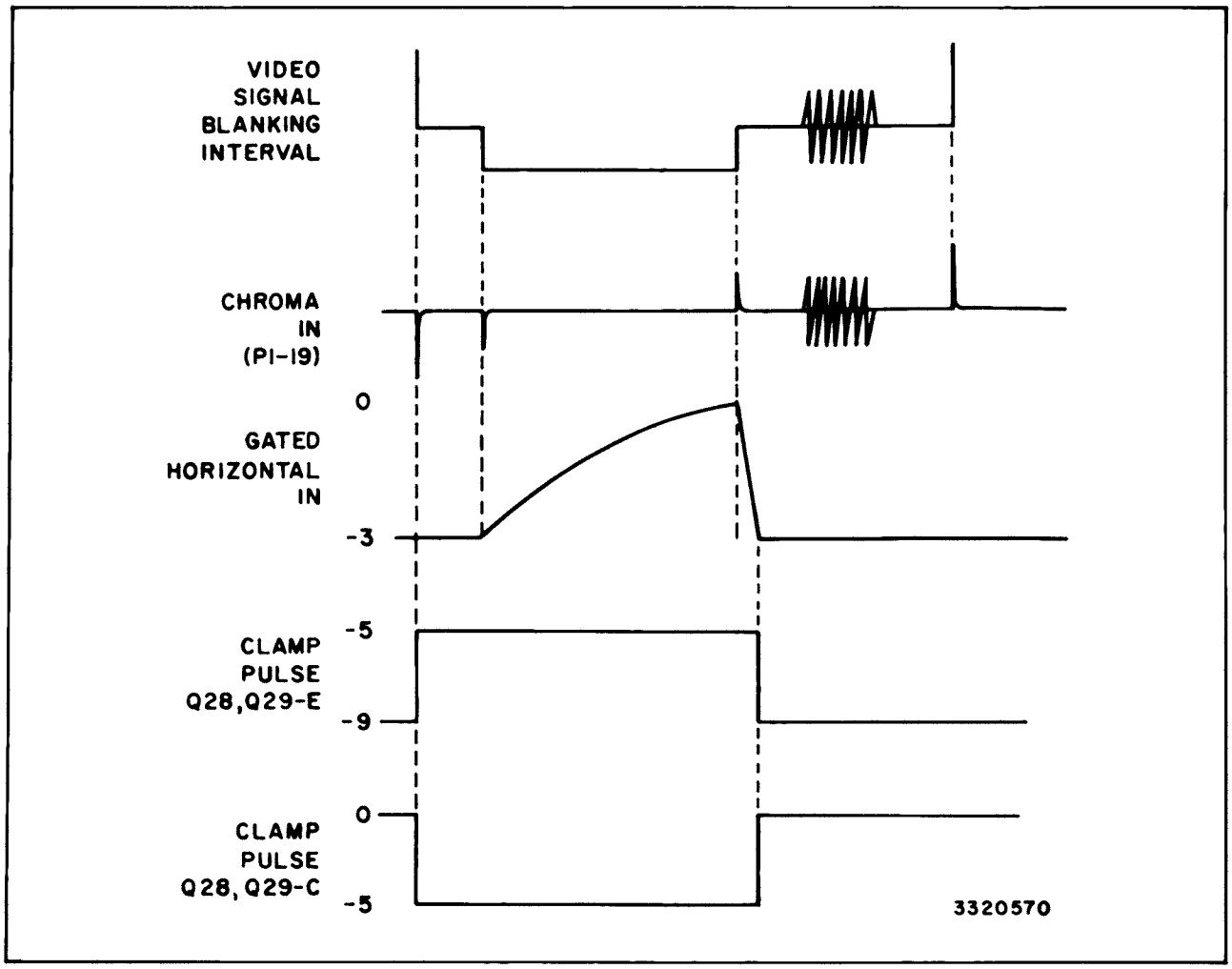
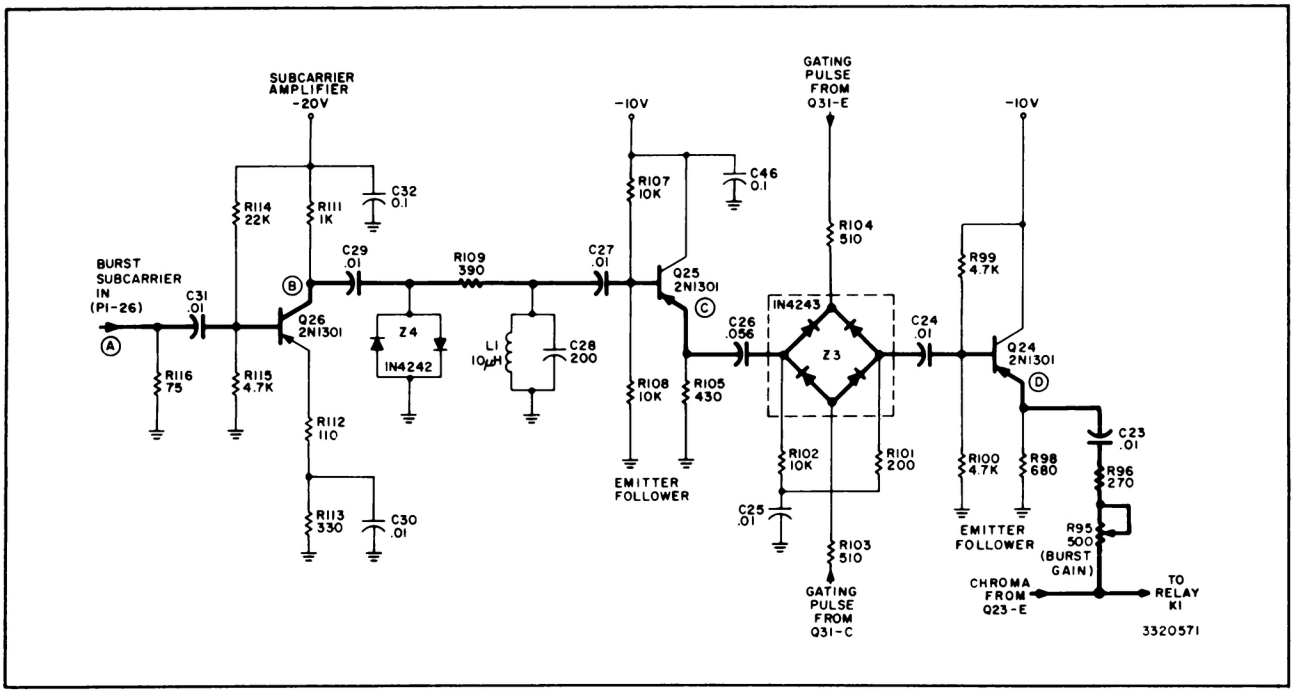


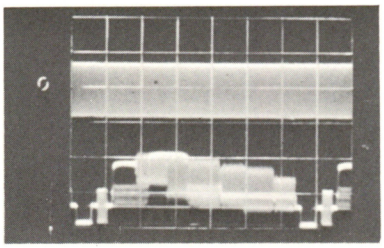
Figure 37—Clamp Pulse Development During Machine Operation in the STOP Mode or During Playback in a Non-Pixlock Servo Mode

Subcarrier Amplifier and Regenerated Burst Separator

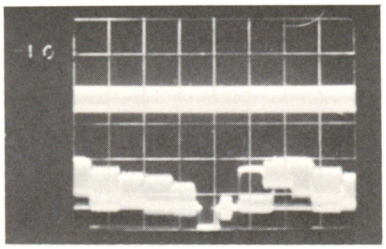
During color tape playback in the pixlock (or linelock) servo mode, the subcarrier amplifier and regenerated burst circuit (figure 38) utilizes a diode quad in separating a portion of the burst subcarrier signal which is obtained from the color phase module. The separated subcarrier signal, constituting regenerated burst, is inserted into the back porch interval of the signal from the chroma separator module, as explained in the *Chroma Amplifier* discussion above, and the resulting chroma signal is fed to color control relay K1. Gating pulses control the diode quad to insure that the proper number of cycles of burst subcarrier are separated and that the separation is timed so that regenerated burst will occur at precisely the correct moment in relation to the remaining portion of the chroma signal (i.e., so that a breezeway interval of 0.5 microsecond will be obtained).

The burst subcarrier signal (figure 38A) is fed to the color processor module at pin 26 of plug P1 from the color phase module (no. 232/C16), and is coupled to amplifier transistor Q26 via capacitor C31. Transistor Q26 is normally biased into conduction by a potential of approximately −4 volts applied to its base from the divider network consisting of resistors R114 and R115. The biasing network in the base circuit of transistor Q26 insures that the incoming subcarrier signal, having an amplitude of approximately 1.5 volts peak-to-peak, will neither saturate nor cut off the transistor. Transistor Q26 provides an a-c gain of approximately 10 to 1, and the amplified signal at its collector is limited by the unitized pair of matched 1N4242 diodes Z4. Each 1N4242 diode has a contact potential of approximately 0.6 volt; therefore, all portions of the amplified subcarrier signal appearing at the collector of transistor Q26 which exceed 0.6 volt in either the positive or

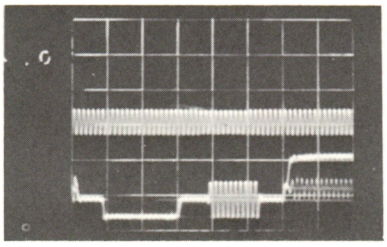




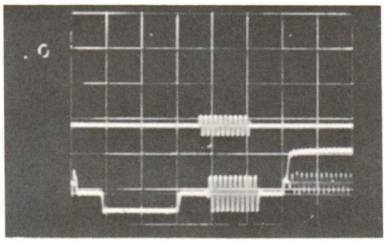
A. Top: Burst SC (P1-26), 1v/cm.
Bottom: Video out (233), 1v/cm.
(10 μsec/cm)



B. Top: Q26 collector, 2v/cm.
Bottom: Video out (233), 1v/cm.
(10 μsec/cm)



C. Top: Q25 emitter, 2v/cm.
Bottom: Video out (233), 1v/cm.
(2 μsec/cm)



D. Top: Q24 emitter, 2v/cm.
Bottom: Video out (233), 1v/cm.
(2 μsec/cm)

Playback in COLOR ATC mode.

Figure 38—Subcarrier Amplifier and Regenerated Burst Separator

the negative direction forward bias one or the other of the diodes and are thereby bypassed to ground. Thus the subcarrier signal fed to emitter follower transistor Q25 is limited in amplitude to approximately 1.2 volts peak-to-peak (figure 38B). Inductor L1 and capacitor C28 form a parallel network which is resonant at the subcarrier frequency and therefore provides a low impedance bypass to ground for all frequency components other than that of the subcarrier.

Transistor Q25, biased into conduction by a potential of approximately −5 volts applied to its base from the divider network consisting of resistors R107 and R108, supplies the current required to drive quad Z3 and isolates the quad from the preceding subcarrier amplifier circuit. The subcarrier signal appearing at the emitter of transistor Q25 (figure 38C) is coupled to quad Z3, which is controlled by burst gating pulses from the emitter and collector of burst gate driver transistor Q31. During the interval between gating pulses, the diodes of the quad are reverse-biased and the quad is cut off. The subcarrier signal appearing at the emitter of transistor Q25 during this interval will therefore be prevented from passing to emitter follower transistor Q24. When the positive- and negative-going burst gating pulses are simultaneously applied to opposite ends of the quad, the quad diodes are forward biased and the subcarrier signal at the emitter of transistor Q25 is coupled to the base of transistor Q24.

The positive- and negative-going burst gating pulses applied to quad Z3 overlap by approximately 3.2 volts, as mentioned below in the *Burst Gate Pulse Generator* discussion, and this potential appears across resistors R103 and R104 in series with the quad. Thus the current flowing through the quad when the gating pulses appear is determined by the voltage developed due to overlapping of the gating pulses and by the values of resistors R103 and R104. These parameters are such that the current flowing through the quad is approximately 3.2 milliamperes. This current exceeds the amplitude of the subcarrier signal current by a sufficient amount to insure that the quad cannot be cut off by normal subcarrier signal current variations during the gating pulse interval.

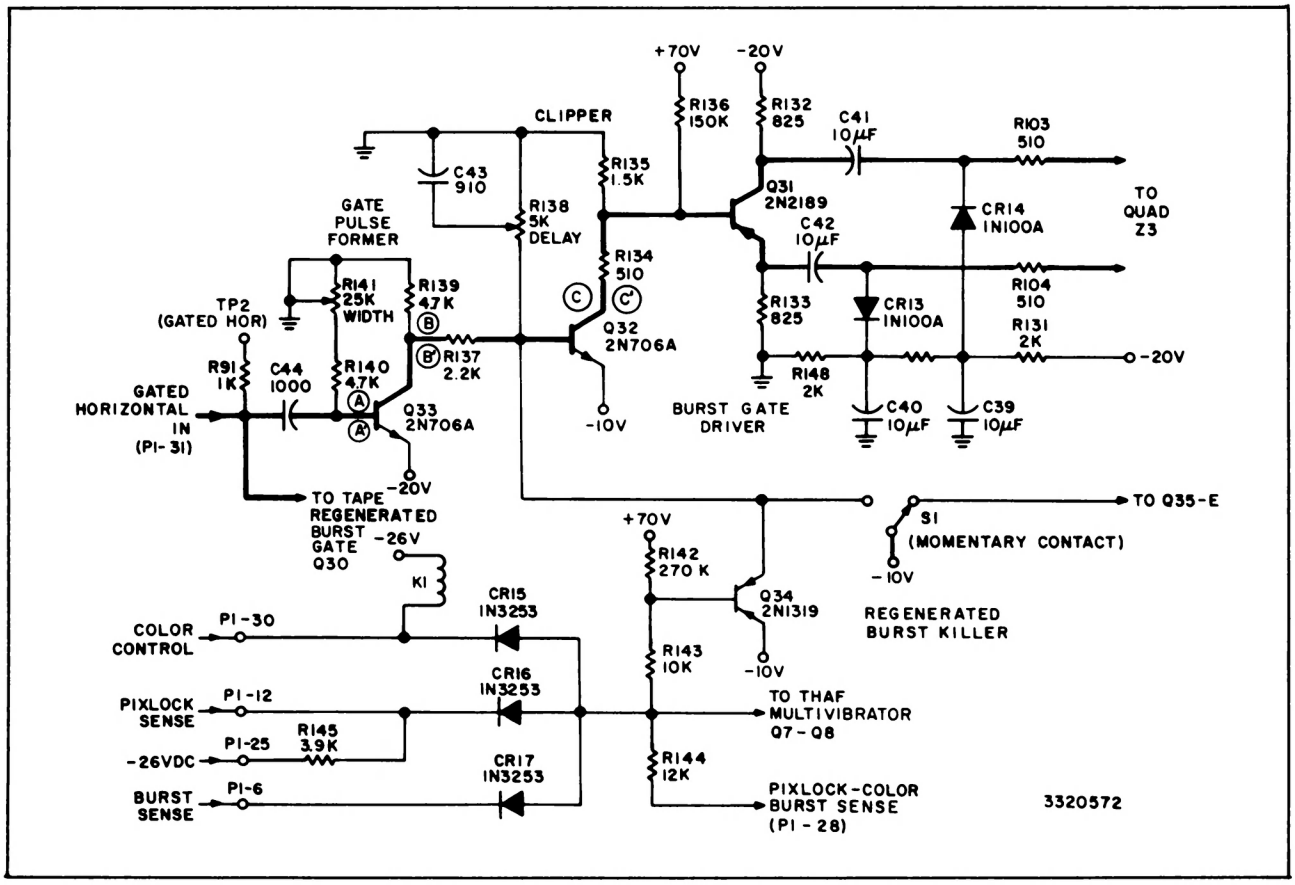
The base potential of emitter follower transistor Q24 is established at approximately −5 volts by the divider network consisting of resistors R99 and R100. Transistor Q24 is biased into conduction by current withdrawn from its base by the negative potential, and the portion of the subcarrier signal passed by quad Z3 appears at its emitter (figure 38D). Transistor Q24 provides the current required to drive the output circuit and isolates the output circuit from the diode quad.

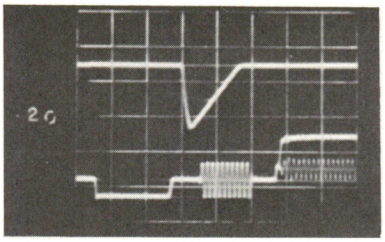
The signal appearing at the emitter of transistor Q24 is the regenerated burst signal which is added to the output signal from emitter follower transistor Q23 in the chroma amplifier circuit. Potentiometer R95 (BURST GAIN) is utilized in setting the level of the regenerated burst signal, and is normally adjusted for a burst amplitude of 0.3 volt as observed in the video output signal from the video output module. (Refer to *Adjustments* at the end of the module circuit description for a BURST GAIN potentiometer adjustment procedure.) The chroma signal containing regenerated burst is applied to relay K1 from which it is fed to the video output module during color tape playback in the normal color ATC or non-phased color mode with the machine "locked" in the pixlock (or linelock) servo mode.

Burst Gate Pulse Generator

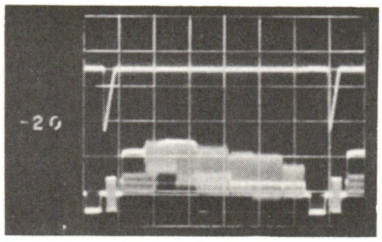
The burst gate pulse generator, shown in figure 39, produces positive- and negative-going gating pulses which control a diode bridge (quad) when the machine is playing back a color tape in the normal color ATC or non-phased color mode with the machine "locked" in the pixlock (or linelock) servo mode. When the gating pulses are applied to the diode quad, the quad passes the portion of burst subcarrier signal utilized as regenerated burst. The burst gating pulses are timed to the leading edge of the gated horizontal pulses, but are delayed slightly to allow for the 'breezeway' interval. Provision is made for varying the width of the burst gating pulses so that approximately 10 cycles of burst subcarrier are passed by the quad during each TV line. Regenerated burst thus produced is added to the back porch interval of the signal obtained from the chroma separator module, as explained in the *Chroma Amplifier* discussion above.

The gated horizontal pulse, developed from tape horizontal sync, is fed to the color processor module via pin 31 of plug P1 from the sync logic module (no. 230/B21) and may be observed at test point TP2 (GATED HOR). The incoming pulse is positive-going and is fed through parallel paths to the tape regenerated burst gate circuit of transistor Q30 and to the gate pulse former circuit of transistor Q33. Capacitor C44 and the series combination of resistor R140 and potentiometer R141 form the timing circuit of boxcar transistor Q33, which is normally saturated by current flowing into its base. The negative-going trailing edge of the gated horizontal pulse drives transistor Q33 into cut-off, and capacitor C44 then begins to discharge toward ground through resistor

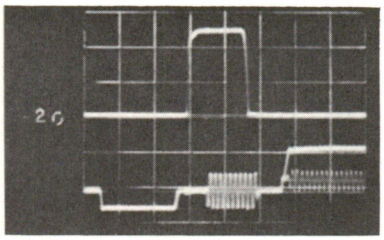




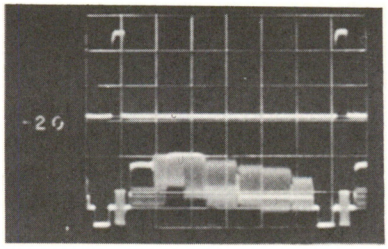
A. Top: Q33 base, 1v/cm.
Bottom: Video out (233), 1v/cm.
(2 μsec/cm)



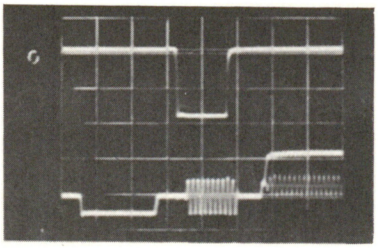
A'. Top: Q33 base, 1v/cm.
Bottom: Video out (233), 1v/cm.
(10 μsec/cm)



B. Top: Q33 collector, 5v/cm.
Bottom: Video out (233), 1v/cm.
(2 μsec/cm)

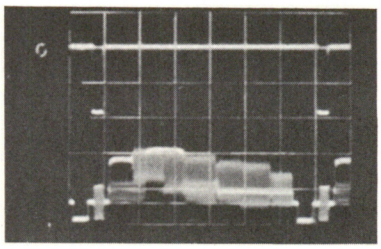


B. Top: Q33 collector, 5v/cm.
Bottom: Video out (233), 1v/cm.
(10 μsec/cm)



C. Top: Q32 collector, 5v/cm.
Bottom: Video out (233), 1v/cm.
(2 μsec/cm)

Playback in COLOR ATC mode.



C'. Top: Q32 collector, 5v/cm.
Bottom: Video out (233), 1v/cm.
(10 μsec/cm)

Figure 39—Burst Gate Pulse Generator and Disabling Circuits

R140 and potentiometer R141 in series. When capacitor C44 has discharged to a potential which is slightly positive with respect to the emitter potential of transistor Q33, the transistor becomes biased into saturation once again (figures 39A and 39A'). As a result of the boxcar action of transistor Q33, a positive-going pulse having a width equivalent to the interval during which Q33 is biased into cut-off appears at its collector (figures 39B and 39B'). Since this interval is determined by the setting of potentiometer R141, which in turn establishes the discharge rate of capacitor C44, the width of the positive-going pulse at the collector of transistor Q33 may be varied by adjusting R141. Potentiometer R141 (WIDTH) is normally adjusted to allow ten cycles of subcarrier signal (regenerated burst) to pass through the diode quad; i.e., for a pulse width of approximately 2.8 microseconds. (Refer to *Adjustments* at the end of the module circuit description.)

The positive-going pulse at the collector of transistor Q33 is integrated by the network consisting of resistor R137, potentiometer R138, and capacitor C43 returned to ground from the center-arm of the potentiometer. The integrated pulse is fed directly to the base of clipper transistor Q32, which is normally biased into cut-off by a potential of approximately −13 volts applied to its base from the divider network consisting of potentiometer R138 and resistor R137 connected between ground and the potential at the collector of transistor Q33. The portion of the integrated pulse which is positive with respect to −10 volts causes current to flow into the base of transistor Q32, thereby biasing the transistor into saturation. Since the setting of potentiometer R138 determines the integration network time constant, and thus the rise time of the leading edge of the integrated pulse, the interval between the leading edge of the pulse at the collector of transistor Q33 and the point at which transistor Q32 is driven into saturation may be varied by adjusting the potentiometer. The resulting signal at the collector of clipper transistor Q32 is a negative-going pulse (figures 39C and 39C') having an amplitude of 10 volts and a leading edge delayed with respect to the gated horizontal pulse trailing edge by an interval which is dependent upon the setting of potentiometer R138. Potentiometer R138 (DELAY) fixes the breezeway interval and is normally adjusted for a breezeway of 0.5 microsecond. (Refer to *Adjustments* at the end of the module circuit description.)

The negative-going pulse appearing at the collector of transistor Q32 is fed to the base of burst gate driver transistor Q31, which is normally biased into cut-off by a potential of approximately +0.7 volt applied to its base from the divider network consisting of resistors R135 and R136 connected between ground and the +70 volt bus. Transistor Q31 is driven into conduction by the negative-going pulse applied to its base and, due to the phase-splitting action of Q31, a negative-going pulse appears at its emitter and a positive-going pulse at its collector. The positive- and negative-going pulses at the collector and emitter respectively of transistor Q31 are designated the regenerated burst gating pulses, and are coupled to quad Z3 where they control the quad diodes. The width of each regenerated burst gating pulse is set by WIDTH potentiometer R141 and the delay of the gating pulse with respect to the gated horizontal pulse is set by DELAY potentiometer R138, as explained in the preceding paragraphs.

Resistors R131, R130, and R148 in conjunction with diodes CR13 and CR14 form a voltage divider which functions as a level-setting network in establishing an 'off' bias of approximately 3.2 volts across quad Z3 during the interval between gating pulses. The amplitude of the positive- and negative-going gating pulses is determined by the drive applied to the base of transistor Q31, and the drive is in turn established by the divider network consisting of resistors R135 and R136. The drive applied to transistor Q31 in conjunction with the levels obtained from the level setting network results in a gating pulse overlap of approximately 3.2 volts. The overlap potential is utilized in developing the current required for proper operation of the quad, as previously explained in the *Regenerated Burst Separator* circuit discussion.

Regenerated burst killer transistor Q34 functions as a switch in disabling the burst gate pulse generator circuit when elimination of the regenerated burst signal is required. The potential applied to the base of transistor Q34 is obtained from an 'AND' gate which is controlled by (1) the color control bus; (2) the pixlock sense bus; and (3) the burst sense bus. During color tape playback in the normal color ATC or non-phased color mode with the machine "locked" in the pixlock (or linelock) servo mode and a normal tape burst signal present, the color control, pixlock sense, and burst sense busses are at ground potential. Diodes CR15, CR16, and CR17 are forward-biased by current supplied by the +70 volt bus via resistors R142 and R143, and the junction of resistors R143 and R144 is at ground potential. A potential of +2.5 volts appears at the base of transistor Q34 from the divider network consisting of resistors R142 and R143, and this potential biases transistor Q34 into

cut-off. Therefore, during normal color tape playback transistor Q34 is cut off and the burst gate generator circuit is allowed to function normally.

When the ATC function selector switch on the monochrome ATC delay/output module front panel is in ATC OFF or COLOR OFF position pin 30 of plug P1 is connected to an open circuit and −26 volts dc is applied to the cathode of diode CR15 from the coil of relay K1. If for any reason the machine has failed to achieve a "lock" in the pixlock (or linelock) servo mode, pin 12 of plug P1 is connected to an open circuit and −26 volts dc is applied to the cathode of diode CR16 via pin 25 of plug P1 and resistor R145. If the tape burst signal is lost for any reason while the machine is otherwise playing back a color tape normally, a burst sense potential of approximately −23 volts dc is applied to the cathode of diode CR17 via pin 6 of plug P1. Therefore, when any or all of the above conditions exist the +70 volt bus supplies current via resistors R142 and R143 which forward-biases the associated 'AND' gate diode(s), and a negative potential appears at the junction of resistors R143 and R144. Transistor Q34 is then biased into saturation by current withdrawn from its base by this potential.

Transistor Q34 is a bilateral type; i.e., either the upper or the lower electrode (in figure 39) may act as emitter or collector, depending upon the biasing potentials. During the interval that gate pulse former transistor Q33 is saturated, the lower electrode of transistor Q34 acts as emitter and the upper as collector. When transistor Q33 is driven into cut-off by the negative-going trailing edge of the incoming gated horizontal pulse its collector potential rises (i.e., becomes more positive) and the upper electrode of transistor Q34 acts as the emitter while the lower electrode acts as the collector. In either case, when transistor Q34 is saturated the base of clipper transistor Q32 is clamped at −10 volts and the burst gate pulse generator circuit is effectively disabled.

Momentary contact pushbutton switch S1 serves the same purpose as regenerated burst killer transistor Q34, and is utilized during normal color tape playback when it is desired to eliminate the regenerated burst signal and observe the original burst signal on the monitor.

In addition to controlling regenerated burst killer transistor Q34, the output potential from the 'AND' gate control circuit is fed via resistor R144 and pin 28 of plug P1 to the color error detector module (no. 326/C14) where it is utilized in controlling the color error clamp circuit.

Adjustments

The color processor module adjustment procedures presented in this section are part of the color ATC system setup adjustments and, with the possible exception of the burst gain potentiometer, once set they should not normally require readjustment. Test equipment required when making the adjustments consists of a vacuum-tube voltmeter such as the *RCA Type WV-98A Voltohmyst,* or the equivalent, and a dual-trace oscilloscope such as the *Tektronix Type 535A* or *Type 545A*, or the equivalent.

General

Where instructions to play back a color test tape are given in this adjustment section, set up the machine as follows:

1a. In TR-22 machines rotate the FM standards switch (module no. 205) to COLOR STD 1 or 2 position; in TR-3 machines rotate the demodulator output switch (module no. A18) to COLOR position; in TR-4 machines rotate both the demodulator output switch and the modulator switch (module nos. A18 and A2) to COLOR position.

b. In all machines rotate the mode selector switch on the ATC delay/output module (no. 223/B11) to COLOR ATC or NON-PHASED COLOR position.

2. Feed a 3.58 mc subcarrier (4.43 mc subcarrier if the machine is operated on 625-line standards) and sync to the machine, and play back a tape containing a color bar signal (split field with 100% white bar) in the pixlock servo mode.

Where instructions are given to operate the machine with a back-to-back signal (MOD-DEMOD mode), set up the machine as follows:

1. In TR-22 machines rotate the FM standards switch (module no. 205) to COLOR STD 1 or 2 position; in TR-3 machines rotate the demodulator output switch (module no. A18) to COLOR position; in TR-4 machines rotate both the demodulator output switch and the modulator switch (module nos. A18 and A2) to COLOR position.

2. In all machines rotate the mode selector switch on the ATC delay/output module (no. 223/B11) to COLOR ATC or NON-PHASED COLOR position.

3. In TR-22 and TR-4 machines feed a color bar signal (split field with 100% white bar), 3.58 mc subcarrier (4.43 mc subcarrier if machine is operated on 625-line standards), and sync to the machine,

and operate the machine in STOP mode (MOD-DEMOD). In TR-3 machines, remove the ATC video out pins (nos. 14 and 30) from the demodulator output module receptacle at the rear of the machine; feed a 1 volt peak-to-peak color signal, subcarrier, and sync to the machine; and operate the machine in the STOP mode.

PEB and NEB

1. Place the color processor module on a module extender, with the board containing potentiometers R64 and R156 facing upward, and operate the machine in the STOP mode.

2. Connect the VTVM between pin 13 of plug P1 and module ground, observing polarity, and adjust potentiometer R156 (DELAY LINE REFERENCE ADJ) for a delay line reference potential of −9.7 volts with respect to ground.

CAUTION: Make certain the VTVM case is insulated from ground when making these adjustments.

3. Connect the VTVM between pin 13 of plug P1 and the base of transistor Q16, and adjust potentiometer R64 (DELAY LINE CENTER) so that the potential at the base of Q16 is +2.9 volts with respect to the delay line reference potential at pin 13.

4. Ground the gamma circuit by connecting a clip lead between the base of transistor Q2 and module ground.

5. Connect the VTVM between pins 13 and 21 of plug P1 and adjust potentiometer R36 (NEB DC SET) for a NEB potential of −0.5 volt with respect to the delay line reference potential.

6. Connect the VTVM between pins 13 and 20 of plug P1 and adjust potentiometer R40 (PEB DC SET) for a PEB potential of +0.5 volt with respect to the delay line reference potential.

7. Remove the clip lead connected in step 4 above.

8. Matrix PEB and NEB potentials at the PEB and NEB test points on the color delay module (no. 324/C12) front panel, utilizing two 20K-ohm, 1%, resistors.

9. A-c couple the external oscilloscope to the matrixed PEB and NEB potentials, and set up the oscilloscope for a 1 millisecond/cm sweep rate ("A" trace) and a .02 volt/cm vertical gain.

10. Set up the machine to play back a color test tape, as instructed in the *General* procedure at the beginning of this adjustment section.

11. Place the vacuum guide in MANUAL mode and decrease the guide pressure.

12. Reduce the monochrome ATC error gain slightly, utilizing the ERR GAIN screwdriver control on the ATC reference module (no. 226/B14) front panel, so that some guide error appears in the color ATC error signal. *Do not exceed the color ATC error signal range.* (In TR-22 machines the color error signal may be observed on the CRO monitor when the CATC ERR pushbutton on the CRO monitor switcher is depressed. In TR-3 or TR-4 machines, the color error signal may be observed by connecting an external oscilloscope probe to the ERR OUT test point on the color error detector module, no. 326/C14, front panel.)

13. Re-adjust potentiometer R40 (PEB DC SET) to minimize 16-line steps.

14. Rotate potentiometers R48 (PEB AC SET) and R44 (NEB AC SET) fully clockwise.

15. Rotate potentiometer R48 counterclockwise until the 16-line spikes are minimized.

16. Increase the vacuum guide pressure.

17. Rotate potentiometer R44 counterclockwise until the 16-line spikes are minimized.

18. Place the machine in the STOP mode.

19. Ground the gamma circuit by connecting a clip lead between the base of transistor Q2 and module ground.

20. Connect the VTVM negative lead to pin 13 of plug P1 (delay line reference), measure the PEB potential at pin 20 and NEB potential at pin 21, and re-adjust potentiometer R156 to split the error difference so that the PEB and NEB potentials are equal and opposite in polarity with respect to the delay line reference potential.

21. With the VTVM negative lead remaining on pin 13 of plug P1, re-adjust potentiometer R36 (NEB DC SET) to obtain a NEB potential at pin 21 of plug P1 equal to −0.5 volt with respect to the delay line reference potential.

22. Remove the clip lead connected in step 19 above.

23. Repeat steps 10 through 13 and, if necessary, steps 14 through 17 above.

24. If potentiometer R40 (PEB DC SET) required re-adjustment in step 23, repeat steps 18 through 24.

25. Reset monochrome ATC error gain screwdriver control (on the monochrome ATC reference module front panel) and vacuum guide control to their normal positions.

Error Signal Centering

NOTE: To properly set the centering controls, all adjustments must first be made according to the procedures outlined above under *PEB* and *NEB*.

1. Place the color processor module on a module extender so that the board containing potentiometer R64 is facing upward.

2. Connect the external oscilloscope probe to pin 17 of plug P1 (ERROR IN), utilizing a 10:1 attenuation probe.

3. Set up the machine to play back a color test tape as instructed in the *General* procedure at the beginning of this adjustment section.

4. Connect the VTVM between pins 20 and 13 of plug P1, and adjust potentiometer R64 (DELAY LINE CENTER) to obtain a PEB potential of +2.9 volts with respect to the delay line reference potential.

5. Adjust the external oscilloscope vertical gain and centering so that the full range of the color ATC error signal (observable during "lock-up") covers 4 cm at the center of the oscilloscope graticule.

6. Adjust potentiometer R7 (SAW CENTERING) so that the average error signal falls at the center of the range established in step 5.

7. Repeat steps 4 and 6.

8. Place the machine in the STOP mode.

9. Place the color error detector module (no. 326/C14) on a second module extender, with the board containing potentiometer R94 facing upward.

NOTE: Since the color processor and color error detector modules are adjacent in TR-3/TR-4 machines, it will not be possible to place both modules on extenders simultaneously. Therefore, in these machines it will be necessary to make trial adjustments in step 10 below until the correct setting of potentiometer R94 is attained.

10. Connect the VTVM between the PEB test point on the color delay module (no. 324/C12) front panel and pin 13 (delay line reference) of plug P1 on the color processor module, and adjust potentiometer R94 (ERR CLAMP SET) in the color error detector module so that the error signal is clamped at a PEB potential of +2.9 volts with respect to the delay line reference potential.

Chroma

1. Place the color processor module on a module extender with the board containing potentiometers R153-R93 and R138-R141 facing upward.

2. Set up the machine for back-to-back (MOD-DEMOD) operation as instructed in the *General* procedure at the beginning of this adjustment section.

3. Connect external oscilloscope probe to the emitter of transistor Q23 and adjust potentiometer R153 (CLAMP BAL) so that the base-line during the vertical interval is aligned with the base-line during the remainder of the field.

4. Connect one of the external oscilloscope probes to the VID 1 test point on the video output module (no. 233/A22) front panel and connect the other probe to the OUT test point on the color delay module (no. 324/C12) front panel.

5. Adjust potentiometer R93 (CHROMA GAIN) so that the chroma amplitude observed at the OUT test point on the color delay module is equal to the chroma amplitude observed at the VID 1 test point on the video output module.

NOTE: It is very important that the various video gain controls be properly set up before setting the chroma gain.

6. Connect a clip lead from pin 12 of plug P1 to module ground.

7. While observing the video signal at the VID 1 test point on the video output module front panel, make the following adjustments:

a. Adjust potentiometer R138 (DELAY) for a 0.5 microsecond breezeway.

b. Adjust potentiometer R141 (WIDTH) for 10 cycles of burst.

c. Adjust potentiometer R95 (BURST GAIN), mounted on the module front panel, for a burst amplitude of 0.3 volt (40 IRE units).

8. Remove the clip lead connected in step 6 and reinsert the color processor module into its receptacle.

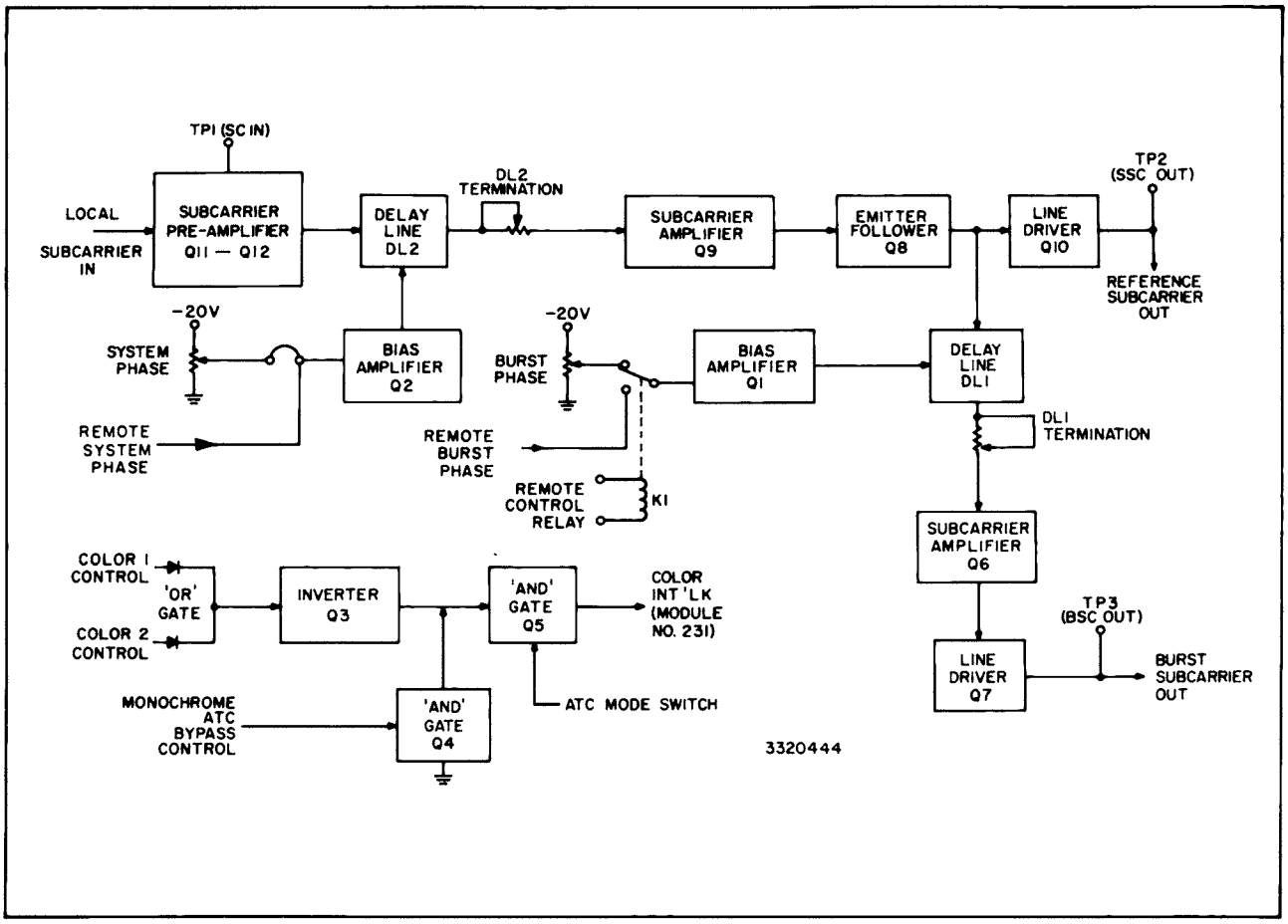


Figure 40—Color Phase Module Block Diagram

COLOR PHASE MODULE (232/C16)

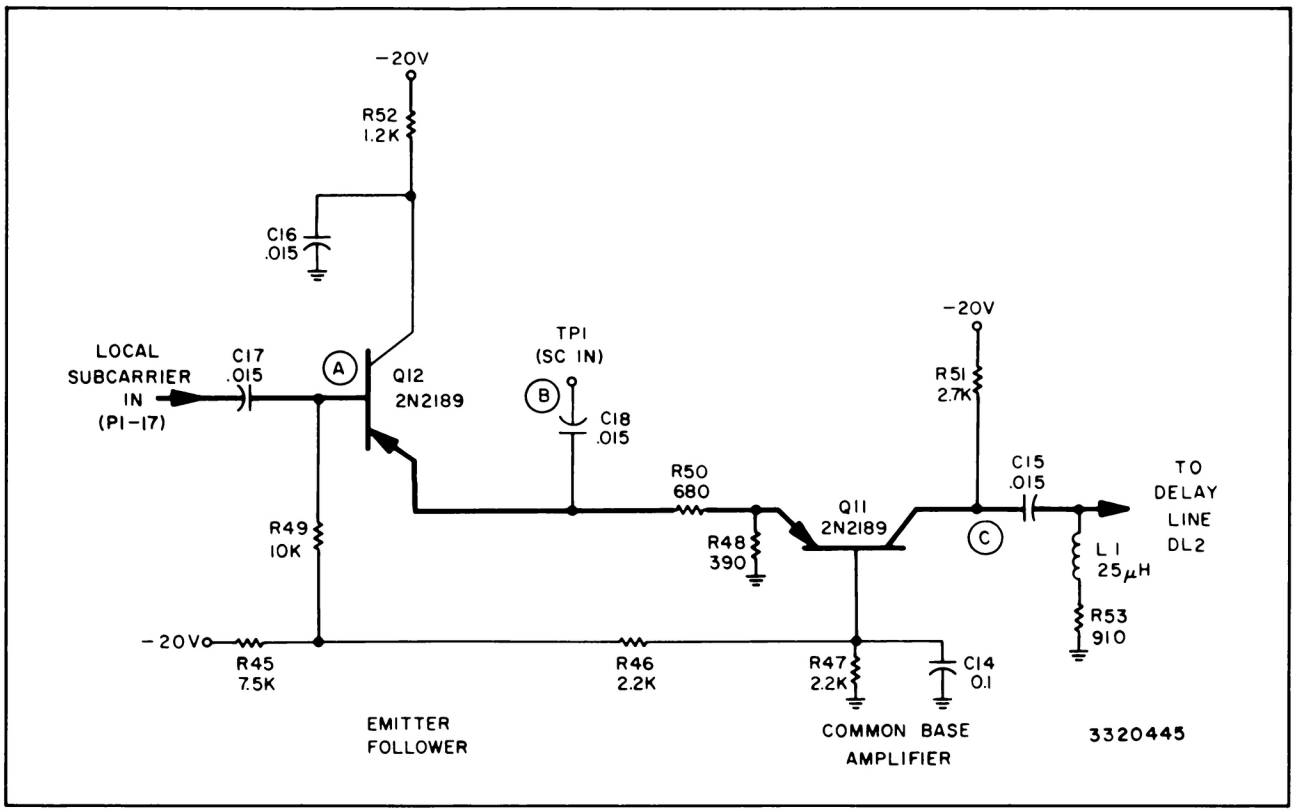
Circuit Description

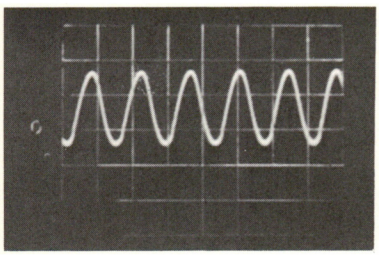
General

The color phase module (no. 232/C16) receives the 3.58 mc subcarrier (4.43 mc in machines operating on 625-line standards) from the local subcarrier signal generator and provides two subcarrier output signals which are utilized in other circuits of the color ATC system. As shown on the block diagram (figure 40), the input subcarrier signal passes through an electronically variable delay line and then splits to form the reference (system) subcarrier and the burst subcarrier signals. The reference subcarrier is fed directly to the color error detector module (no. 326/C14) where it is processed and developed into a reference sawtooth waveform. The burst subcarrier is passed through a second electronically variable delay line before being fed to the color processor module (no. 231/C15) where it is utilized in the development of regenerated burst.

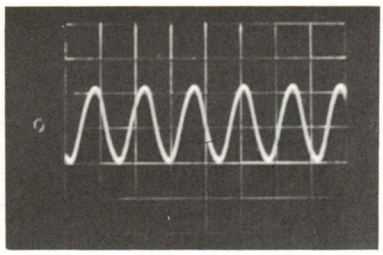
The delay of each delay line is continuously variable over a range of nominally 0.3 microsecond (i.e., a subcarrier phase shift in excess of 360 degrees) by means of the SYSTEM PHASE and BURST PHASE controls which are located on the module front panel. These controls are the only operating controls in the color ATC system. Provision is made for remote operation of the controls with only minor circuit modifications.

Also included in the color phase module is a logic circuit consisting of an 'OR' gate (in TR-22 machines) and two 'AND' gates. The function of this circuit is to provide a ground potential, when certain operating conditions are satisfied, which is interlocked through the remaining color ATC system modules and then fed to the color bypass relays and to the color processor module.

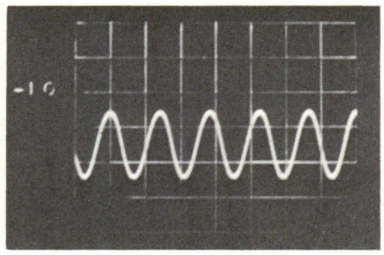




A. Q12 base, 1v/cm.



B. TP1 (SC IN), 1v/cm.



C. Q11 collector, 0.5v/cm.

Machine in STOP mode (back-to-back signal). All sweep times 0.2 μsec/cm.

Figure 41—Local Subcarrier Preamplifier

Subcarrier Preamplifier

Transistors Q11-Q12 and associated circuit components form the subcarrier preamplifier circuit (figure 41). This circuit is essentially an emitter follower driving a common base amplifier. The emitter follower (transistor Q12) provides a high input impedance to reduce the loading effect on the incoming local subcarrier signal, and the common base amplifier (transistor Q11) acts as a current source in providing the current required to drive the input terminating impedance of delay line DL2.

The local subcarrier is a 3.58 mc sinusoidal signal (4.43 mc in machines operating on 625-line standards) obtained from the local station subcarrier signal generator, and is fed to the color phase module at pin 17 of plug P1. The incoming subcarrier signal, shown in figure 41A, is capacitance coupled to the base of emitter follower transistor Q12. The subcarrier signal at the emitter of Q12 may be observed at test point TP1 (SC IN). (See figure 41B.)

Transistors Q11 and Q12 receive biasing potentials from a common bleeder network consisting of resistors R45, R46, and R47 so that variations in component values and power supply levels will cause

their operating points to shift simultaneously. The steady state current flowing in both transistors Q11 and Q12 also flows through resistor R48. The signal current at the emitter of transistor Q11 is then equal to the peak-to-peak voltage of the signal appearing at the emitter of transistor Q12 divided by resistor R50, and the output voltage at the collector of Q11 (figure 41C) is equal to that current times the load impedance which in turn is determined by resistors R51 and R53 in parallel and delay line DL2. In installations where the local subcarrier amplitude is substantially less than the standard 2 volts peak-to-peak, it is possible to change the gain of the stage by reducing the value of resistor R50 so that the amplitude of the subcarrier signal fed to the delay line is equal to that of a normal installation. Resistors R51 and R53 in parallel form a 680-ohm source impedance which matches the 680-ohm characteristic impedance of the delay line.

Delay Line DL2 and Reference Subcarrier Output Amplifier

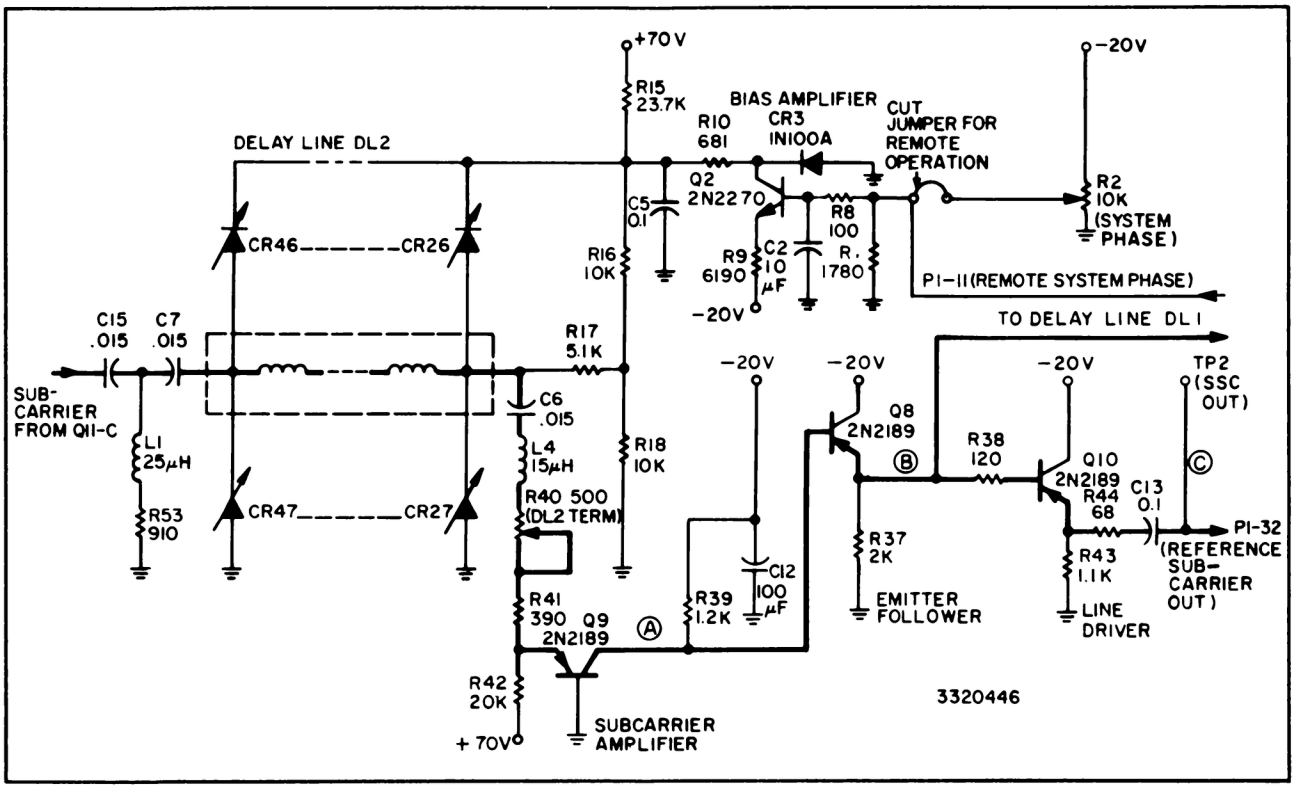
The sinusoidal signal appearing at the collector of transistor Q11 is capacitance coupled to the electronically variable delay line DL2 (figure 42). Delay line DL2 contains variable capacitance diodes (*Varicaps*) whose capacitance varies inversely with the magnitude of the d-c potential impressed across them. E.g., as the d-c potential decreases, the capacitance of the diodes (and thus the delay) increases. The magnitude of the potential impressed across the diodes depends upon the degree of conduction of bias amplifier transistor Q2, and the conduction of Q2 is in turn controlled by varying potentiometer R2 (SYSTEM PHASE). When potentiometer R2 is varied over its entire range, a change of delay in excess of 0.28 microsecond (equivalent to 360 degrees of subcarrier phase shift) will be obtained.

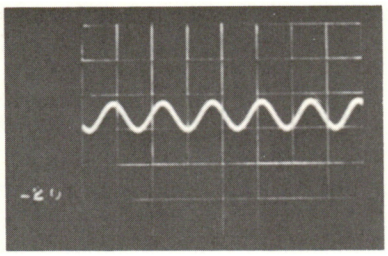
Bias amplifier transistor Q2, an NPN type, conducts when its base potential is positive with respect to that at its emitter. The base potential of transistor Q2 is determined by the setting of potentiometer R2 (SYSTEM PHASE control), as shown in figure 42. When potentiometer R2 is rotated fully clockwise, the base potential of transistor Q2 is −20 volts and, due to the biasing arrangement in its emitter circuit, the transistor is cut off. As potentiometer R2 is rotated in a counterclockwise direction, the potential at the base of transistor Q2 rises toward ground and Q2 begins to conduct. When potentiometer R2 is rotated fully counterclockwise, the base of transistor Q2 is essentially at ground potential and Q2 is then saturated. Thus the potential at the collector of transistor Q2 varies between the approximate limits of +32 volts and ground as potentiometer R2 is rotated over its full range in a counterclockwise direction. Diode CR3, in the collector circuit of transistor Q2, prevents the collector potential from going more negative than the contact potential of the diode (approximately +0.2 volt).

When transistor Q2 is cut off, a potential of +32 volts appears at the junction of resistors R15 and R16 in the voltage divider network consisting of resistors R15, R16, and R18. The full +32 volts is impressed across delay line DL2 and one half of this voltage (+16 volts) appears at the mid-point of the delay line. Under these conditions the capacitance of the diodes in the delay line is at a minimum and, since the delay of the line varies as the square root of the diode capacitance, the delay presented by DL2 is also at a minimum. As potentiometer R2 is varied so that the potential at the base of transistor Q2 approaches ground, Q2 conducts more heavily and its collector potential also approaches ground. This action reduces the potential across the delay line, thereby causing an increase in diode capacitance and thus an increase in delay. When transistor Q2 becomes saturated, the potential at the junction of resistors R15 and R16 is reduced to approximately +1.7 volts and maximum delay is attained.

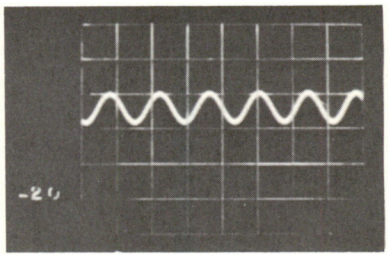
Thus the SYSTEM PHASE control (potentiometer R2) is utilized in varying the delay of delay line DL2 over a range which corresponds to a subcarrier phase shift of at least 360 degrees. In the color system the SYSTEM PHASE control acts as a cable length compensating device and its purpose is to make it possible to precisely adjust the phase of the system subcarrier signal so that when mixing various color signal sources the phase of each is identical with respect to that of a reference. Provision is made for remote operation of the SYSTEM PHASE control, and the modifications required for this purpose are outlined in the *Installation* section of this instruction book.

The delayed subcarrier signal from DL2 is fed through the series network containing capacitor C6, inductor L4, and a termination resistance consisting of resistor R41 and potentiometer R40. Capacitor C6 is utilized as a d-c blocking capacitor. Inductor L4 acts as a frequency compensating device which counteracts the natural capacitive reactance of the delay line and thus causes the line to appear resistive so that a smooth termination may be obtained. Termination potentiometer R40 is then utilized in actually obtaining the smooth termination by impedance matching and thus minimizing reflections.

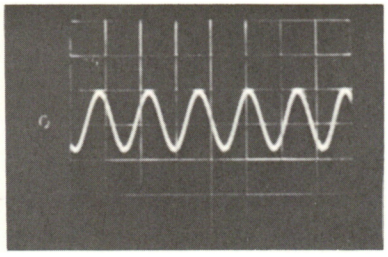




A. Q9 collector, 1v/cm.



B. Q8 emitter, 2v/cm.



C. TP2 (SSC OUT), 0.5v/cm.

Machine in STOP mode (back-to-back signal). All sweep times 0.2 μsec/cm.

Figure 42—System Subcarrier Delay and Output Circuits

IMPORTANT: The delay line termination potentiometer setting is critical. Since the potentiometer has been factory adjusted for optimum delay line performance, it is important that the setting not be disturbed.

Common base amplifier transistor Q9, acting as an impedance transformer, amplifies the delayed subcarrier signal, and the amplitude of the signal at its collector is approximately 0.9 volt peak-to-peak (figure 42A). The signal at the collector of transistor Q9 is then fed directly to the base of emitter follower transistor Q8. Transistor Q8 isolates delay line DL2 from the succeeding circuitry, and the sinusoidal subcarrier signal at the emitter of Q8 (figure 42B) is fed simultaneously to the output driver transistor Q10 and to delay line DL1. The function of delay line DL1 is discussed below. Driver transistor Q10 operates as an emitter follower and provides the current gain required to drive the system (reference) subcarrier output. The system subcarrier output signal (figure 42C) may be observed at test point TP2 (SSC OUT), and is fed via pin 32 of plug P1 to the color error detector module (no. 326/C14) where it is utilized in the development of a reference sawtooth waveform.

Delay Line DL1 and Burst Subcarrier Output Amplifier

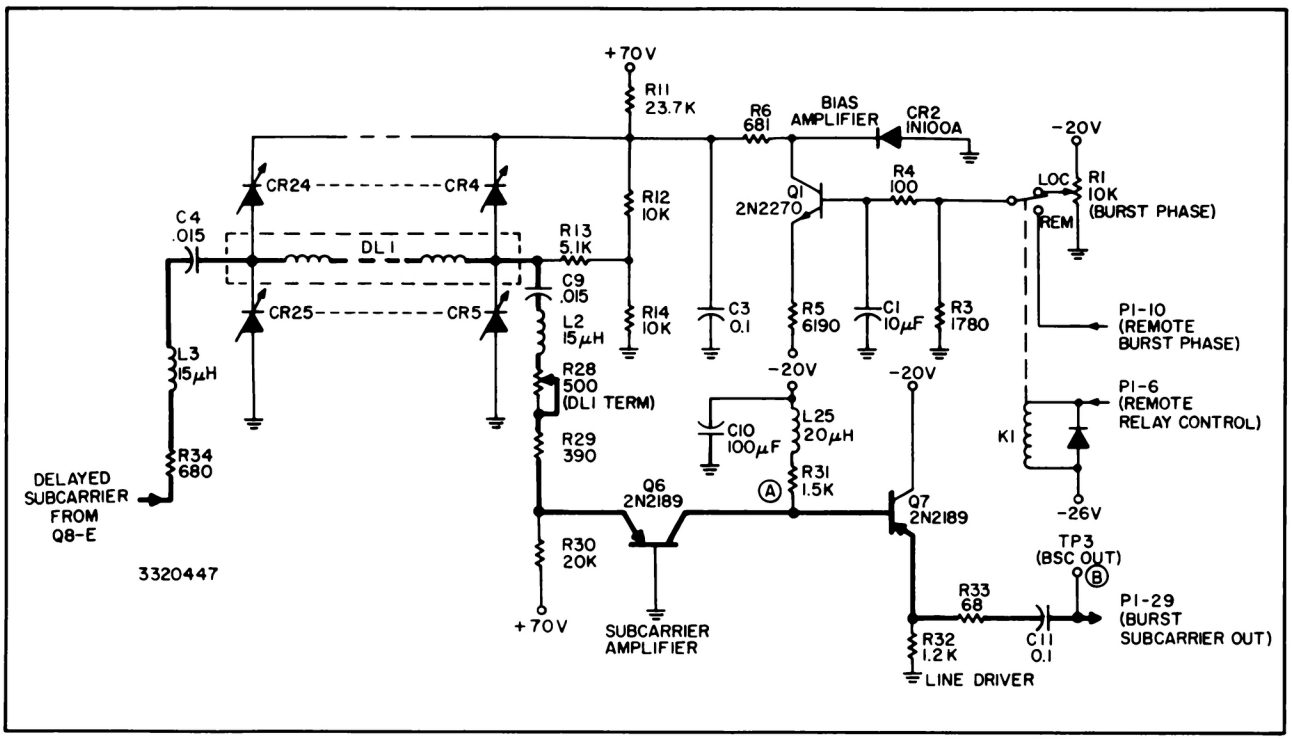
The portion of the subcarrier signal at the emitter of transistor Q8 which is fed to electronically variable delay line DL1 is designated the burst subcarrier signal. Delay line DL1 operates in a manner identical to that of delay line DL2 (figure 43). As explained above in the discussion of delay line DL2, the capacitance of the delay line silicon diodes depends upon the magnitude of the d-c potential impressed across them, and this potential is in turn controlled by a bias amplifier transistor. Bias amplifier transistor Q1 operates similarly to bias amplifier transistor Q2; i.e., the transistor conducts more heavily as its base potential becomes increasingly positive with respect to that at its emitter. The base potential of transistor Q1 is determined by the setting of potentiometer R1 (BURST PHASE control). When potentiometer R1 is rotated fully clockwise, the base potential of transistor Q1 is −20 volts and, due to the biasing arrangement in its emitter circuit, the transistor is cut off. As potentiometer R1 is rotated in a counterclockwise direction, the potential at the base of transistor Q1 rises toward ground and Q1 begins to conduct. When potentiometer R1 is rotated fully counterclockwise, the base of transistor Q1 is essentially at ground potential and Q1 is then saturated. Thus the potential at the collector of transistor Q1 varies between the approximate limits of +32 volts and ground as potentiometer R1 is rotated over its full range in a counterclockwise direction. Diode CR2, in the collector circuit of transistor Q1, prevents the collector potential from going more negative than the contact potential of the diode (approximately +0.2 volt).

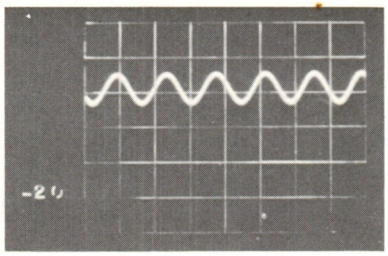
When transistor Q1 is cut off, a potential of +32 volts appears at the junction of resistors R11 and R12 in the voltage divider network consisting of resistors R11, R12, and R14. The full +32 volts is impressed across delay line DL1 and one half of this voltage (+16 volts) appears at the mid-point of the delay line. Under these conditions the capacitance of the diodes in the delay line is at a minimum and, since the delay of the line varies as the square root of the diode capacitance, the delay presented by DL1 is also at a minimum. As potentiometer R1 is varied so that the potential at the base of transistor Q1 approaches ground, Q1 conducts more heavily and its collector potential also approaches ground. This action reduces the potential across the delay line, thereby causing an increase in diode capacitance and thus an increase in delay. When transistor Q1 becomes saturated, the potential at the junction of resistors R11 and R12 is reduced to approximately +1.7 volts and maximum delay is obtained.

Thus the BURST PHASE control (potentiometer R1) is utilized in varying the delay of delay line DL1 over a range which corresponds to a subcarrier phase shift of at least 360 degrees. In the color system the BURST PHASE control is utilized in adjusting the system to obtain a proper color picture, containing natural flesh tones, etc. Relay K1 controls the local/remote burst phase control option. Normally, relay K1 is deenergized and the burst phase is then controlled locally (at the module front panel). If the proper connections are made for remote operation (refer to the *Installation* section), a ground potential appears at pin 6 of plug P1 when the LOCAL/REMOTE pushbutton (located on the TR-22 machine RECORD control panel or on the TR-3/TR-4 machine playback control panel) is pressed for remote control. The ground potential energizes relay K1 (figure 43) and thereby delegates control of the burst phase to the remote location.

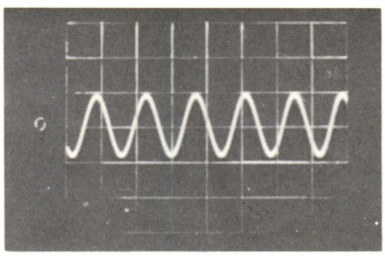
NOTE: Certain modifications are possible which will enable relay K1 to delegate control of the system phase as well as the burst phase to a remote location. These modifications are also outlined in the *Adjustment* section of this instruction book.

The delayed burst subcarrier signal from DL1 is fed through the series network containing capacitor C9, inductor L2, and a termination resistance consisting of resistor R29 and potentiometer R28. Capacitor





A. Q6 collector, 1v/cm.



B. TP3 (BSC OUT), 1v/cm.

Machine in STOP mode (back-to-back signal). All sweep times 0.2 μsec/cm.

Figure 43—Burst Subcarrier Delay and Output Circuits

C9 is utilized as a d-c blocking capacitor. Inductor L2 acts as a frequency compensating device which counteracts the natural capacitive reactance of the delay line and thus causes the line to appear resistive so that a smooth termination may be obtained. Termination potentiometer R28 is then utilized in actually obtaining the smooth termination by impedance matching and thus minimizing reflections.

IMPORTANT: The delay line termination potentiometer setting is critical. Since the potentiometer has been factory adjusted for optimum delay line performance, it is important that the setting not be disturbed.

Common base amplifier transistor Q6, acting as an impedance transformer, amplifies the delayed burst subcarrier signal, and the amplitude of the signal at its collector is approximately 0.9 volt peak-to-peak (figure 43A). The signal at the collector of transistor Q6 is then fed directly to the base of emitter follower transistor Q7. Transistor Q7 isolates delay line DL1 from the succeeding circuitry, and provides the current required to drive the burst subcarrier output signal. The burst subcarrier output signal (figure 43B) may be observed at test point TP3 (BSC OUT), and is fed via pin 29 of plug P1 to the color processor module where it is utilized in the regeneration of burst.

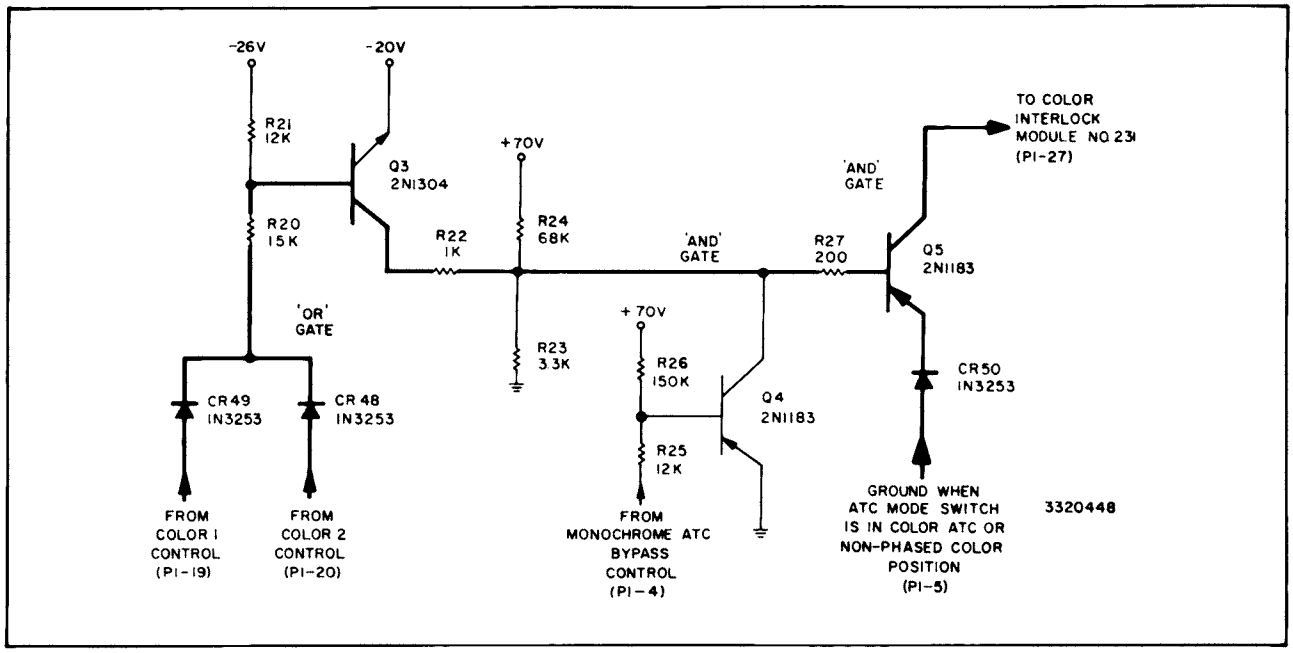


Figure 44—Control Circuit

Control Circuit

The control circuit consists of an 'OR' gate (required by TR-22 machines only) and two 'AND' gates, as shown in figure 44. The purpose of the control circuit is to operate in conjunction with the color module interlock in inhibiting the operation of the color ATC system under the following conditions:

(1) FM standards switch (module no. 205) in TR-22 machines or demodulator output switch (module no. A18) in TR-3/TR-4 machines in any position except COLOR.

> NOTE: In TR-22 machines, the FM standards switch has two positions (COLOR STD 1 and COLOR STD 2). The COLOR STD 2 position is for use in special applications; e.g. high band, where different deviations are utilized.

(2) ATC mode switch (module no. 223/B11) in ATC OFF or COLOR OFF position.

(3) Any ATC module (monochrome or color) not securely inserted into its receptacle.

If any of the above conditions prevail, the COLOR/BYPASS relays will be deenergized and the color ATC system is then removed from the signal path. (Refer to the *System Functional Description* section for a complete explanation of the color ATC control system.)

Transistor Q3, an NPN type, is saturated when the potential at its base is positive with respect to its emitter potential. The base potential of transistor Q3 depends upon the condition of diodes CR48 and CR49, and the diodes in turn are controlled by the switch on the FM standards module (no. 205) front panel. (See *Note* below.) When the FM standards switch is in COLOR STD 1 position, ground potential is applied via pin 19 of plug P1 to the anode of diode CR49 and the diode is forward biased. Similarly, when the FM standards switch is in COLOR STD 2 position, ground potential is applied via pin 20 of plug P1 to the anode of diode CR48 and the diode is forward biased. Diodes CR48 and CR49 form the 'OR' gate, and when either diode is forward biased the divider network consisting of resistors R20 and R21 is returned to ground potential. The potential applied to the base of transistor Q3 is then positive with respect to the −20 volts at the emitter of Q3 and the transistor is driven into saturation. A potential of approximately −20 volts appears at the collector of transistor Q3 when Q3 is saturated, and this results in a negative potential at the junction of resistors R23 and R24. When transistor Q4 is cut off, the negative potential is applied through current limiting resistor R27 to the base of transistor Q5.

When the FM standards switch is in MONO STD 1, 2, or 3 position, ground potential is not supplied to the anode of either of the 'OR' gate diodes and the diodes are in effect cut off. In this case, −26 volts is applied to the base of transistor Q3 via resistor R21 and, since this potential is negative with respect to the −20 volts at the emitter of Q3, the transistor is cut off. Then, when transistor Q4 is also

cut off, a positive potential appears at the junction of resistors R23 and R24 and is fed to the base of transistor Q5.

NOTE: The above discussion of the 'OR' gate circuit pertains to color ATC system operation in TR-22 machines. In TR-3/TR-4 machines the standards switch is on the demodulator output module (no. A18) and has only two positions (MONO and COLOR). In this case only diode CR49 is controlled by the switch position. The remaining portions of the circuit description pertain to color ATC system operation in TR-3/TR-4 machines as well as in TR-22 machines.

The emitter of transistor Q5 is connected to the cathode of diode CR50, and the anode of the diode is connected via pin 5 of plug P1 to pin 12 of plug P1 in the ATC delay/output module (no. 223/B11). Pin 12 of plug P1 in the ATC delay/output module is connected via diodes to the COLOR ATC and NON-PHASED COLOR positions of the ATC mode switch in such a manner that when the mode switch is in either COLOR ATC or NON-PHASED COLOR position ground potential is applied to the anodes of the diodes and the diodes are forward biased. This places the emitter of transistor Q5 at approximately ground potential and a negative potential at its base will drive the transistor into saturation. When transistor Q5 is saturated, a ground potential appears at its collector. The ground potential at the collector of transistor Q5 is fed directly to pin 27 of plug P1, interlocked through the remaining color ATC modules, and applied to the color bypass relays and to relay K1 in the color processor module (no. 231/C15).

Note that transistor Q5 can become saturated only when transistor Q4 is cut off and transistor Q3 is saturated. When transistor Q4 is saturated, the base of transistor Q5 is clamped at ground potential and Q5 cannot possibly conduct. The condition of transistor Q4 (either cut off or saturated) depends upon the potential applied to pin 4 of plug P1. If the ATC mode switch on the ATC delay/output module is in COLOR OFF, COLOR ATC, or NON-PHASED COLOR position, and all ATC modules are securely in place, pin 4 of plug P1 is at ground potential. This results in the application of a positive bias potential to the base of transistor Q4 from the voltage divider network consisting of resistors R25 and R26, and Q4 is cut off. The ground potential at pin 4 of plug P1 is also fed to the ATC bypass relays and, in TR-22 machines, to the ATC indicator lamp thus causing it to become illuminated. When any conditions prevail other than those mentioned above which are required to obtain a ground potential at pin 4, the ATC indicator lamp is extinguished and a potential of −26 volts dc is applied to pin 4 via the ATC bypass relay coils. The −26 volts at pin 4 causes a negative potential to appear at the base of transistor Q4 from the voltage divider network consisting of resistors R25 and R26. The negative potential drives Q4 into saturation, and its collector is then essentially at ground potential. When transistor Q4 is saturated, the base of transistor Q5 is clamped at ground potential and Q5 is cut off.

Thus it may be seen that several conditions must prevail in order to obtain a ground potential at pin 27 of plug P1. These conditions are (1) the switch on the FM standards module (no. 205) must be in either COLOR STD 1 or COLOR STD 2 position (TR-22 machines) or, the switch on the demodulator output module (no. A18) must be in COLOR position (TR-3/TR-4 machines); (2) the ATC mode switch on the ATC delay/output module must be in COLOR ATC or NON-PHASED COLOR position; and (3) the monochrome ATC modules must be securely inserted into their respective receptacles. Under any other conditions, pin 27 is essentially an open circuit. (In addition to the above conditions, the color ATC modules must be securely inserted into their respective receptacles for the ground potential at pin 27 to energize the color bypass relays.)

Adjustments

Burst Phase

Adjust the BURST PHASE control to obtain a proper color picture in the following manner:

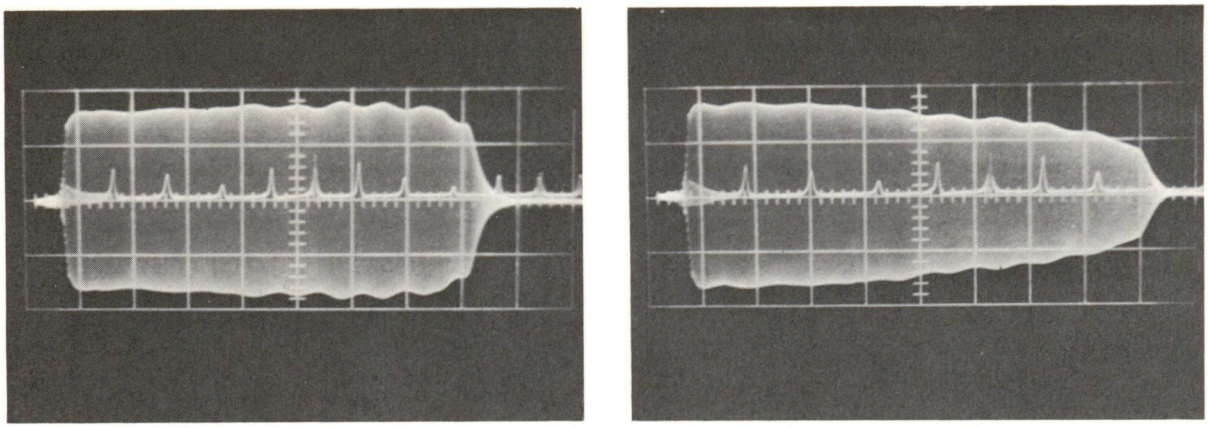
Play back a color bar signal and adjust the BURST PHASE control so that color bars appearing on the color monitor with the VID OUT pushbutton on the picture monitor switcher depressed are identical in shading to the color bars appearing on the monitor when the VID IN pushbutton is depressed.

System Phase

Adjust the SYSTEM PHASE control when mixing various color signal sources (e.g., live and tape color signals) so that the phase of each source is identical with respect to that of a reference.

Delay Line Termination Potentiometers

Termination potentiometers R28 and R40 have been factory adjusted for optimum color ATC performance and should require no further adjustment. In the event that one or both of the potentiometers become inadvertently misadjusted, an emergency procedure for re-adjusting the potentiometer(s) is given below. Test equipment required consists of the following:



A. System SC out (P1-32).

B. Burst SC out (P1-29).

Figure 45—Delay Line Output Waveforms with Sweep Input

75-ohm Attenuator

Video Sweep Generator (*Marconi Model 1099* or equivalent)

Dual-Trace Oscilloscope (*Tektronix Type 535A*, or *Type 545A* with CA plug in, or equivalent)

Vacuum-tube Voltmeter (*RCA Voltohmyst* or equivalent)

NOTE: Before making any adjustments it is advisable to mark the present potentiometer setting by some convenient means (e.g., a scribe mark on the shaft).

1. Disconnect coax cables from jacks J5 and J6 (SC IN) on the connection board at the bottom of the machine, and connect a 75-ohm termination plug to either J5 or J6. (In TR-3/TR-4 machines the SC IN jacks are designated J3 and J4 and are located at the rear of the machine.)

2. Connect the video sweep generator output to the jack which has not been terminated.

3. Connect the oscilloscope trigger input to the time base terminal of the sweep generator.

4. Place the color phase module on the module extender.

5. Connect one of the oscilloscope probes to the local subcarrier input of the color phase module (at the junction of capacitor C17 and the coax cable from pin 17 of plug P1).

6. Connect the other oscilloscope probe to the sweep generator marker output.

7. Set the sweep generator for a sweep width out to 15 mc, and adjust the generator output for an amplitude of 2.0 volts peak-to-peak as observed on the oscilloscope.

8. Remove the oscilloscope probe from the subcarrier input and connect it to test point TP2 (SSC OUT).

9. Adjust the SYSTEM PHASE control, on the module front panel, to the center of its range.

10. While observing the oscilloscope, adjust the delay line termination potentiometer R40 (DL2 TERM) to minimize ripples in the response.

11. Check the response with the SYSTEM PHASE control adjusted to positions near the extremes of its range. The final adjustment of termination potentiometer R40 should be that which results in the lowest ripple over the entire range of the SYSTEM PHASE control. Ripple should not exceed 5% of the signal amplitude to 7.0 mc, and the frequency response should not be down more than 10% at 7.0 mc in comparison with that at 1.0 mc. (See figure 45A.)

NOTE: If the response exhibits excessive ripple, the delay line is faulty. Due to the complexity of repair techniques, the RCA Service Company should be consulted if it is determined that the delay line is faulty.

12. Remove the oscilloscope probe from test point TP2 and connect it to test point TP3 (BSC OUT). Repeat steps 9, 10, and 11, utilizing the BURST PHASE control and delay line termination potentiometer R28 (DL1 TERM). (See figure 45B.)

13. Disconnect the sweep generator and attenuator plug and re-connect the coax cables to jacks J5 and J6 (J3 and J4 in TR-3/TR-4 machines).

14. Re-insert the color phase module into its receptacle.

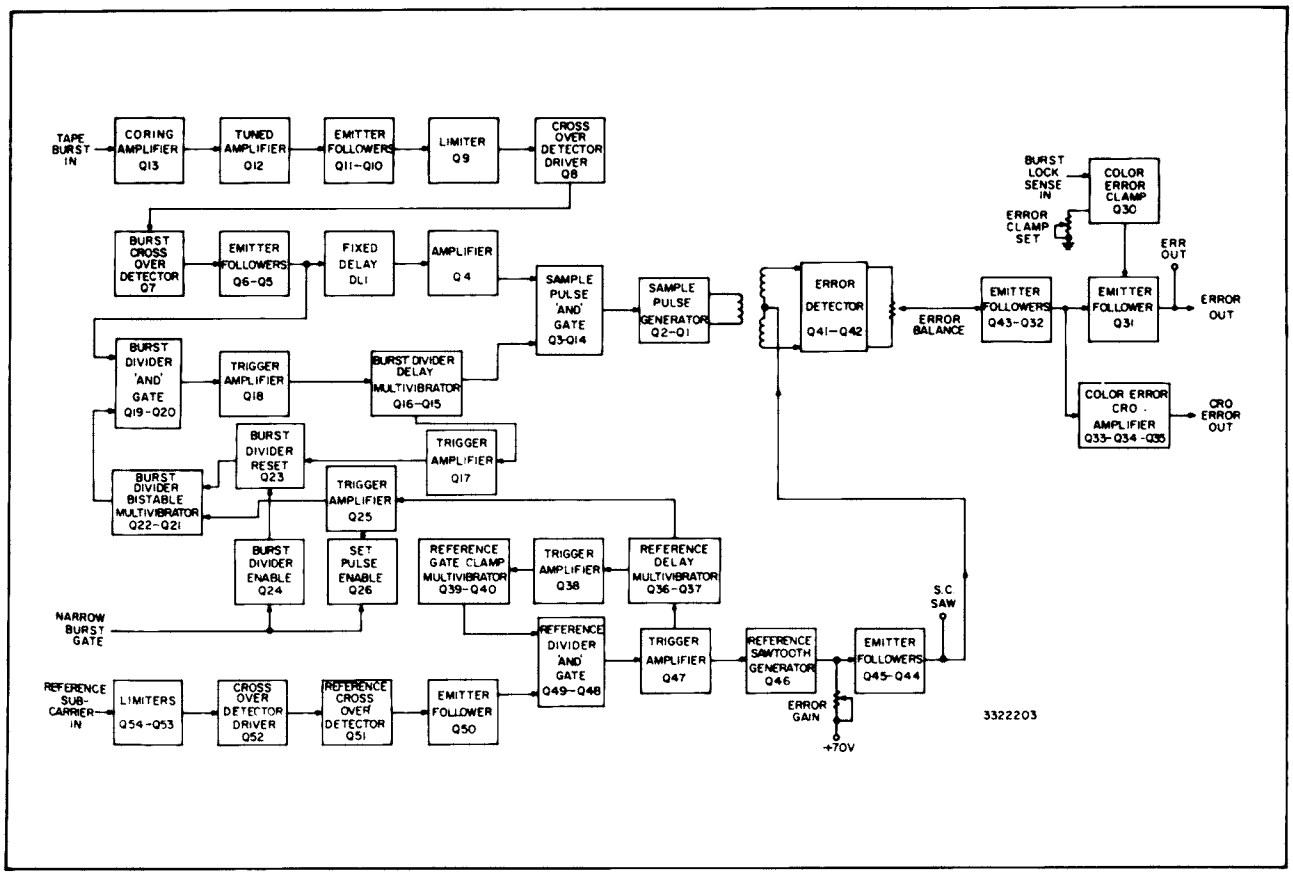


Figure 46—Color Error Detector Module Block Diagram

COLOR ERROR DETECTOR MODULE (326/C14)

Circuit Description

General

The color error detector module (no. 326/C14) is shown in block diagram form in figure 46. The primary function of this module is to provide the phase error signal utilized in the color processor module (no. 231/C15) in developing the PEB (positive error bus) and NEB (negative error bus) potentials which in turn control the delay developed by the video delay line in the color delay module (no. 324/C12) during tape playback in the color ATC mode.

The error signal developed by the color error detector circuitry is a function of the difference in phase between the tape burst signal and the reference subcarrier signal. The method of error detection employed consists of sampling the slope of a sawtooth waveform derived from the reference subcarrier signal with a pulse derived from the tape burst signal. Logic circuits insure that sampling will occur only over the linear portion of the sawtooth waveform slope, and therefore the gain of the error detector will be linear. The slope of the sawtooth waveform, and thus the gain of the circuit, may be varied by adjusting the COLOR ERR GAIN potentiometer located on the module front panel. In TR-22 machines, provision is made for monitoring the error detector output on the CRO monitor.

The reference subcarrier logic circuit produces a 70 nanosecond pulse, occurring at one-half the reference subcarrier frequency. The leading edge of the 70 nanosecond pulse, timed to the point at which the reference subcarrier signal crosses the zero axis in a positive-going direction, is utilized in generating the reference sawtooth waveform. Thus the reference sawtooth waveform occurs at one-half the reference subcarrier rate, and the base of its slope is timed to the reference subcarrier crossover point. The delayed (trailing) edge of the 70 nanosecond pulse is utilized in generating a triggering pulse which "sets" the burst divider bistable multivibrator in the burst logic circuit.

The incoming tape burst signal is passed through coring and tuned amplifier circuits which produce a regenerated burst signal and thus minimize the possibility of an erroneous error signal being generated

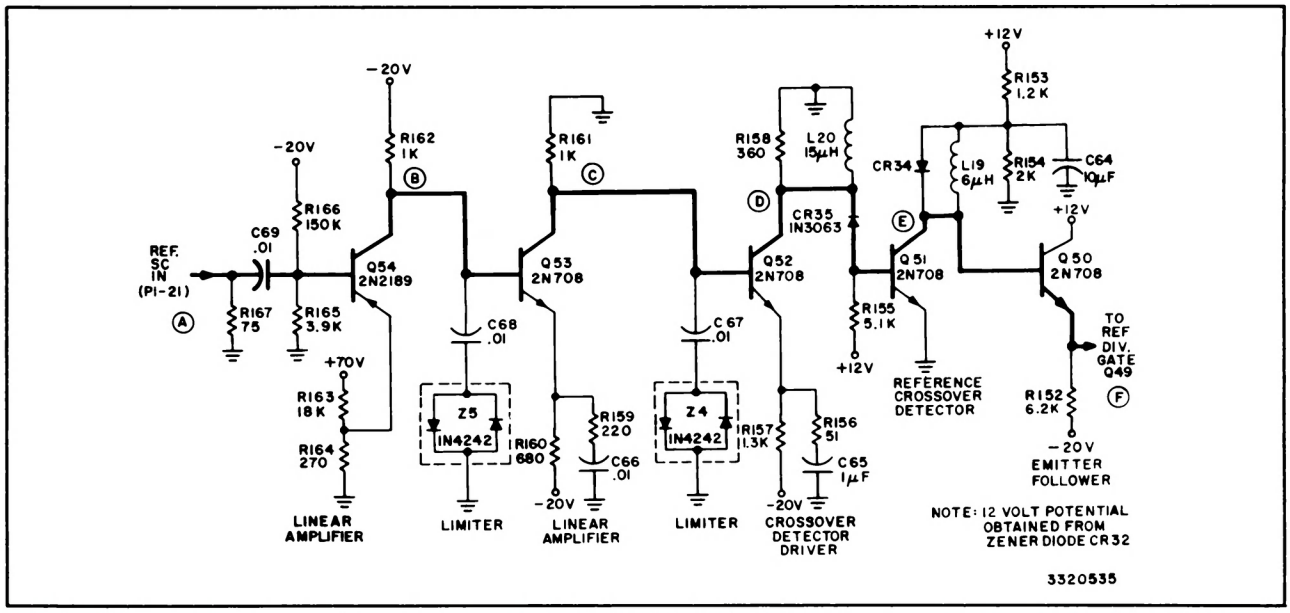
due to noise or other spurious signals appearing in the tape burst. The regenerated burst signal follows parallel paths to a logic circuit utilized in developing the phase sample pulse. One of the parallel paths contains a fixed delay which delays the regenerated burst signal 70 nanoseconds. The other path contains the burst logic circuit which produces a 140 nanosecond pulse having a leading edge timed to the point at which the burst signal crosses the zero axis in a positive-going direction and a frequency equal to one-half that of the tape burst signal.

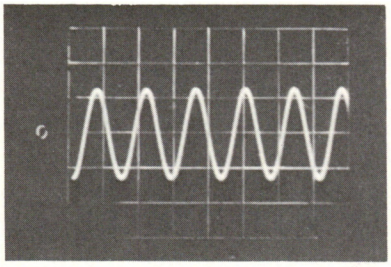
The heart of the burst logic circuit is the burst divider bistable multivibrator. The bistable multivibrator is set by a pulse derived from the trailing edge of the 70 nanosecond pulse developed in the reference subcarrier logic circuit, and is re-set by a pulse derived from the trailing edge of the 140 nanosecond pulse developed in the burst logic circuit itself. Thus the bistable multivibrator output signal bears a definite relationship to both the reference subcarrier and the tape burst signals. It is this relationship then which insures that the sample pulse will sample only on the desired portion of the sawtooth waveform slope. Enabling circuits gated by the narrow burst pulse developed in the chroma separator module (no. 325/C13) control the bistable multivibrator set and reset pulses so that the burst logic circuit will produce an output only during the narrow burst gating interval. The duration of the narrow burst gating interval may be varied by adjusting the BURST GATE WIDTH potentiometer in the chroma separator module, and an average potentiometer setting results in an interval of approximately 2.4 microseconds. Therefore, since the period of the 140 nanosecond burst logic pulse is approximately 0.56 microsecond, approximately five 140 nanosecond pulses will be produced during each TV line.

The sample pulse logic circuit is gated by the 140 nanosecond pulse developed in the burst logic circuit and produces a sample pulse when the delayed pulse developed from regenerated burst appears during the gating interval. Therefore the sample pulse occurs at one-half the tape burst frequency and is delayed 70 nanoseconds with respect to the leading edge of the 140 nanosecond pulse (i.e., advanced 70 nanoseconds with respect to the trailing edge of the 140 nanosecond pulse from which the burst divider bistable multivibrator reset pulse is derived). The sample pulse is combined with the reference sawtooth waveform in the pulse transformer secondary winding, and the combined signal is fed to the error detector circuit.

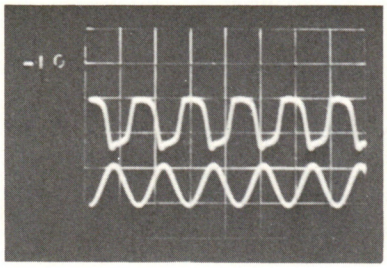
The timing of the burst divider bistable multivibrator set pulse insures that the sample pulse cannot occur prior to 70 nanoseconds after the beginning of the sawtooth waveform slope and the fixed delay in the sample pulse logic circuit adds another 70 nanoseconds; thus the sample pulse cannot occur until at least 140 nanoseconds after the beginning of the sawtooth waveform slope. Similarly, the timing of the bistable multivibrator reset pulse is such that the sample pulse cannot occur later than 350 nanoseconds after the earliest possible sampling point (i.e., 490 nanoseconds after the beginning of the sawtooth waveform slope). Thus sampling is made to occur over the linear portion of the sawtooth waveform slope and the gain of the error detector circuit is linear. If the sample pulse is sampling near either extreme of its range on the sawtooth waveform slope it is possible to obtain the "cracking effect" (i.e., successive pulses sampling at alternate extremes of the slope and thus producing conflicting error information). To prevent this effect during normal tape playback in the color ATC mode, a portion of the phase error signal is utilized in controlling the THAF (tape horizontal alignment, fine) signal in the color ATC system and the THAF signal in turn adjusts the video delay slightly so that the sample pulse will sample near the center of the sawtooth waveform slope. (The cracking effect may be created artificially by operating the machine in the STOP mode with a back-to-back color signal and adjusting the SYSTEM PHASE control on the color phase module front panel until cracking occurs.)

Approximately five samplings are obtained during each TV line (depending upon the width of the narrow burst gating pulse), and the potential on the waveform slope at the instant of sampling is impressed across a storage capacitor. The storage capacitor retains its charge between sampling intervals and the output error signal is a fluctuating series of d-c potentials. Since normal error signal development requires the presence of a tape burst signal, absence of tape burst could result in an undesirable erratic output from the error detector circuitry. To eliminate the possibility of an erratic output signal, a clamping circuit provides a steady d-c output signal which corresponds to zero error if for any reason there is no tape burst signal. Therefore, signal fluctuations which may occur in the error detector circuit due to the lack of a normal tape burst signal will not affect the PEB and NEB potentials and thus will not affect the video delay line.

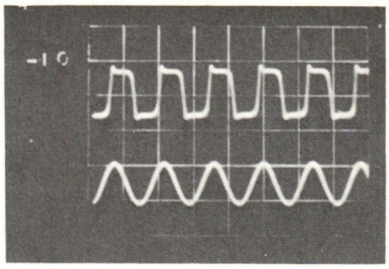




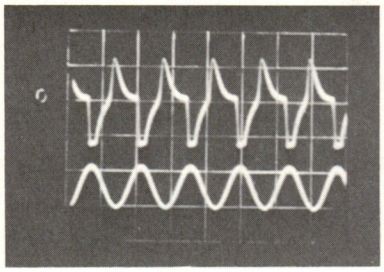
A. Reference SC (P1-21), 0.5v/cm.



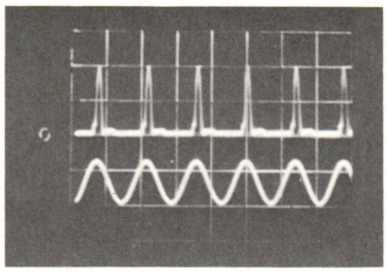
B. Top: Q54 collector-Q53 base, 1v/cm.
Bottom: Reference SC (P1-21), 1v/cm.



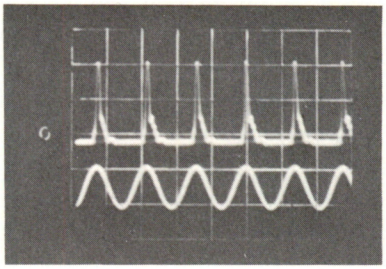
C. Top: Q53 collector-Q52 base, 1v/cm.
Bottom: Reference SC (P1-21), 1v/cm.



D. Top: Q52 collector, 2v/cm.
Bottom: Reference SC (P1-21), 1v/cm.



E. Top: Q51 collector, 2v/cm.
Bottom: Reference SC (P1-21), 1v/cm.



F. Top: Q50 emitter, 2v/cm.
Bottom: Reference SC (P1-21), 1v/cm.

Machine in STOP mode (back-to-back signal). All sweep times 0.2 μsec/cm.

Figure 47—Reference Subcarrier Limiter and Crossover Detector Circuits

Reference Subcarrier Limiter and Crossover Detector Circuits

The reference subcarrier signal fed to the color error detector module is the local 3.58 mc subcarrier (4.43 mc subcarrier in machines operating on 625-line standards) which has been shifted in phase by an electronically variable delay line in the color phase module (no. 232/C16). The amount that the reference subcarrier signal has been shifted in phase with respect to the local subcarrier signal depends upon the setting of the SYSTEM PHASE control on the color phase module front panel.

The incoming reference subcarrier signal, having an amplitude of approximately 1 volt peak-to-peak as shown in figure 47A, is coupled from pin 21 of plug

P1 to the base of linear amplifier transistor Q54. The base potential of transistor Q54 is approximately −0.5 volt due to the voltage divider action of resistors R166 and R165 connected between the −20 volt bus and ground. The divider network consisting of resistors R163 and R164 connected between the +70 volt bus and ground in the emitter circuit of transistor Q54 establishes an emitter potential which is positive with respect to the base potential and the transistor is biased into conduction. The biasing potentials of transistor Q54 are such that a normal incoming sinusoidal subcarrier signal will neither drive the transistor into saturation nor cut it off; therefore the gain of the transistor (approximately 4 to 1) is linear.

The signal at the collector of amplifier transistor Q54 is limited by limiter Z5. Limiter Z5 is a unitized pair of matched 1N4242 diodes, each having a contact potential of approximately 0.6 volt. Since limiter Z5 is returned to a-c ground, all portions of the signal at the collector of transistor Q54 which exceed 0.6 volt in either a positive or a negative direction will be bypassed to ground through the diodes. Therefore the signal fed to the base of transistor Q53 has an amplitude of approximately 1.2 volts peak-to-peak and appears as shown in figure 47B.

A d-c potential of approximately −15 volts is applied to the base of transistor Q53 and the transistor is biased into conduction by current withdrawn from its base. Transistor Q53, functioning as a linear amplifier in the same manner as transistor Q54, provides a signal gain of approximately 6 to 1, and the signal at its collector is further limited by limiter Z4 which operates in exactly the same manner as limiter Z5. Thus the signal at the base of transistor Q52 approaches a square wave with an amplitude of approximately 1.2 volts peak-to-peak and a sharp positive-going edge (figure 47C).

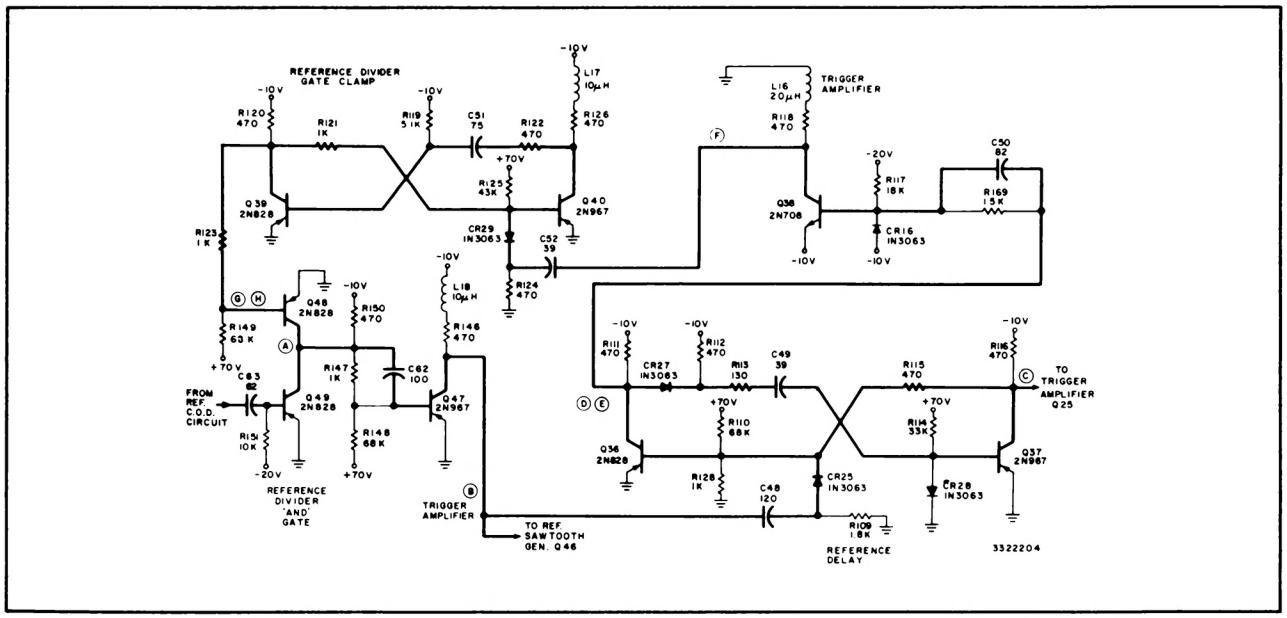
Transistor Q52 functions as the crossover detector driver, and a d-c potential of approximately −7 volts applied to its base causes a base current to flow which biases the transistor into conduction. The square wave signal fed to the base of transistor Q52 is differentiated by the parallel combination of resistor R158 and inductor L20 in the collector circuit of Q52. The differentiation network has the effect of amplifying the high frequency components (sharp edges) of the signal fed to transistor Q52, whereas inductor L20 provides a low impedance path to ground for the lower frequency signal components. Therefore, due to a polarity inversion and the differentiation action, the signal at the collector of transistor Q52 has a sharp negative-going edge and an amplitude of approximately 5 volts peak-to-peak as shown in figure 47D.

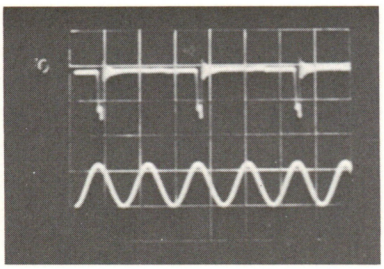
The negative-going spikes at the collector of driver transistor Q52 are fed via diode CR35 to the base of reference crossover detector transistor Q51. Positive-going spikes appearing at the collector of transistor Q52 reverse-bias diode CR35 and therefore do not appear at the base of transistor Q51. Transistor Q51 is normally biased into saturation by current flowing into its base from the +12 volt bus via resistor R155, and the sharp negative-going spikes fed to its base then drive the transistor into cut-off.

During the interval that reference crossover detector transistor Q51 is saturated, its collector is at ground potential. When transistor Q51 is driven into cut-off by the negative-going edge of the waveform fed to its base, its collector voltage rises toward a potential of +7.5 volts established by the divider network consisting of resistors R153 and R154 connected between +12 volts and ground, but is prevented from reaching this level by the action of inductor L19. Inductor L19 would normally have a "ringing" effect in the collector circuit of transistor Q51; however, after the positive-going half-cycle of the waveform occurs, the negative-going half-cycle forward biases diode CR34, thus bypassing the inductor, and the remainder of the waveform is effectively damped out. Therefore, due to the action of inductor L19 and diode CR34, the signal at the collector of transistor Q51 is a positive-going pulse which occurs at the subcarrier frequency and has an amplitude of approximately 4 volts as shown in figure 47E.

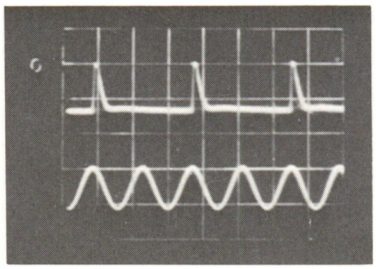
The high frequency peaking action of inductor L19 insures that the reference crossover detector output pulse will have a rapid positive-going (leading) edge, and it is this edge which bears a definite phase relationship to the subcarrier crossover point (i.e., the point at which the reference subcarrier sine wave crosses the zero axis in a positive-going direction). Therefore, regardless of the amount that the reference subcarrier signal may be shifted in phase, the *difference* in phase between the subcarrier crossover point and the rapid positive-going edge of the pulse at the collector of transistor Q51 will remain constant.

Transistor Q50, biased into conduction by the current withdrawn from its base, functions as an emitter follower in providing the current gain required to drive transistor Q49 in the reference divider gate circuit. The positive-going crossover detector pulse at the emitter of transistor Q50 is shown in figure 47F.

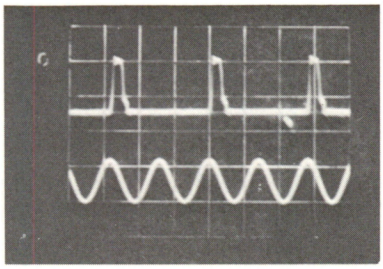




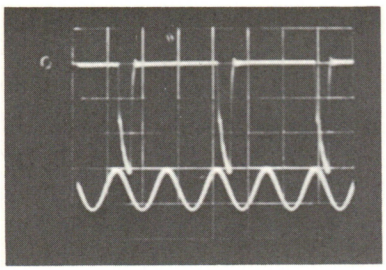
A. Top: Q48 collector, 2v/cm. Bottom: Reference SC (P1-21), 1v/cm.



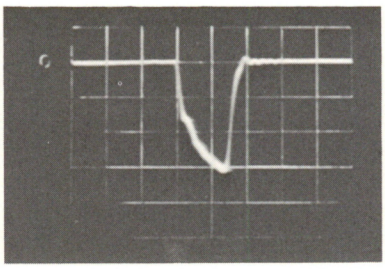
B. Top: Q47 collector, 5v/cm. Bottom: Reference SC (P1-21), 1v/cm.



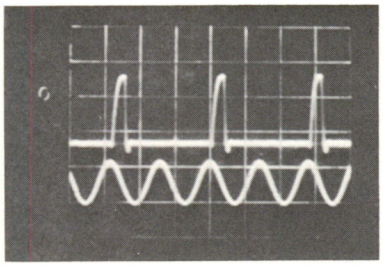
C. Top: Q37 collector, 2v/cm. Bottom: Reference SC (P1-21), 1v/cm.



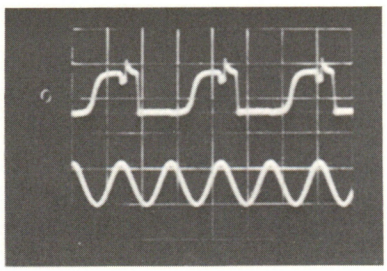
D. Top: Q36 collector, 2v/cm. Bottom: Reference SC (P1-21), 1v/cm.



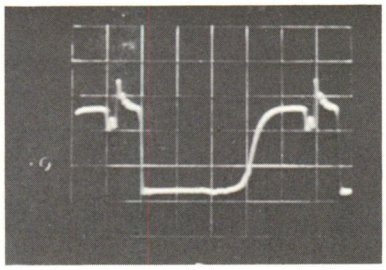
E. Q36 collector, 2v/cm. (.05 μsec/cm)



F. Top: Q38 collector, 5v/cm. Bottom: Reference SC (P1-21), 1v/cm.



G. Top: Q48 base, 1v/cm. Bottom: Reference SC (P1-21), 1v/cm.



H. Q48 base, 0.5v/cm. (0.1 μsec/cm)

Machine in STOP mode (back-to-back signal). All sweep times 0.2 μsec/cm unless otherwise noted.

Figure 48—Reference Subcarrier Divider and Delay Circuit

Reference Subcarrier Divider and Delay Circuit

The purpose of the reference subcarrier divider and delay circuit is to divide the frequency of the incoming reference C.O.D. (crossover detector) pulse by two, and to thereby produce two individual pulses which occur at one-half the subcarrier rate. Frequency division is accomplished by employing a closed loop circuit wherein a divider gate is controlled by the output from a monostable multivibrator which is in turn triggered by a pulse derived from the divider gate output. (Refer to figure 48.) One of the pulses produced by this circuit is utilized in generating the reference sawtooth waveform, while the second pulse is utilized in the burst divider bistable multivibrator circuit. The pulse utilized in the burst divider bistable multivibrator circuit requires a positive-going edge delayed by 70 nanoseconds with respect to the positive-going timed edge of the reference C.O.D. pulse. The 70 nanosecond delay is attained by employing a monostable multivibrator which is designed especially for producing a very narrow pulse while at the same time maintaining rapid (sharp) pulse edges.

The incoming signal fed to transistor Q49 in the reference divider 'AND' gate circuit is the reference C.O.D. pulse which has a sharp positive-going edge and occurs at the subcarrier rate. Transistor Q49 is normally biased into saturation by the current withdrawn from its base, and the common collector of transistors Q48-Q49 is then clamped at ground potential. The positive-going reference C.O.D. pulse drives transistor Q49 into cut-off. Since the reference divider 'AND' gate transistors Q48 and Q49 have a common collector circuit, their common collector potential depends upon the state of both transistors. As mentioned above, transistor Q49 is normally saturated. Transistor Q48, however, is normally biased into cut-off by the positive potential applied to its base when the monostable gate clamp multivibrator Q39-Q40 is in its stable state. Therefore, during stable conditions (i.e., during the interval between reference C.O.D. pulses) the common collector of transistors Q48-Q49 is clamped at ground potential.

When the positive-going reference C.O.D. pulse drives transistor Q49 into cut-off, and transistor Q48 is held in cut-off by the gate clamp multivibrator Q39-Q40, the common collector potential of transistors Q48-Q49 falls to approximately -2.5 volts due to the voltage divider action of resistors R150 and R147 in conjunction with the fact that trigger amplifier transistor Q47 is then biased into saturation (as explained below). However, monostable gate clamp multivibrator Q39-Q40 is triggered into its timed cycle (unstable state) during the interval between every second reference C.O.D. pulse (as explained below), and during the multivibrator timed cycle transistor Q48 is biased into saturation by current withdrawn from its base. As is the case with transistor Q49, when transistor Q48 is biased into saturation the common collector of transistors Q48-Q49 is clamped at ground potential. Therefore, transistors Q48 and Q49 are both cut off only upon the occurrence of every second reference C.O.D. pulse. The resulting output at the common collector of transistors Q48-Q49 (figure 48A) is a negative-going pulse having a frequency equal to one-half that of the reference subcarrier and a negative-going edge which is timed to the positive-going edge of the reference C.O.D. pulse. (See timing diagram, figure 49.)

As mentioned above, reference divider 'AND' gate transistor Q49 is normally biased into saturation and the common collector of transistors Q48-Q49 is clamped at ground potential. A positive potential of approximately 1 volt then appears at the base of trigger amplifier transistor Q47, due to the voltage divider action of resistors R147 and R148 connected between ground and $+70$ volts, and transistor Q47 is biased into cut-off. When a negative-going pulse appears in the common collector circuit of transistors Q48 and Q49, the base potential of transistor Q47 is driven negative with respect to ground by the action of the voltage divider network consisting of resistors R148, R147, and R150 connected between $+70$ volts and -10 volts. Transistor Q47 is thereby driven into saturation and its base, and thus the junction of resistors R147 and R148, is clamped at ground potential. Ground potential at the junction of resistors R147 and R148 in turn results in a potential of approximately -2.5 volts at the common collector of transistors Q48-Q49; thus the amplitude of the negative-going divided reference subcarrier pulse is held at approximately -2.5 volts.

Trigger amplifier transistor Q47 inverts and amplifies the divided reference subcarrier pulse (figure 48B), and the positive-going leading edge of the pulse at the collector of Q47 is timed to the positive-going leading edge of the reference C.O.D. pulse. Inductor L18 is utilized as a peaking coil which aids in amplifying the high frequency components of the trigger pulse, thus insuring a sharp positive-going edge. The positive-going triggering pulse at the collector of transistor Q47 is fed to the reference delay multivibrator (discussed below) and to transistor Q46 in the reference sawtooth generator circuit.

Transistors Q36-Q37 and associated circuit components form a monostable reference delay multivibrator. In the multivibrator stable state, transistor

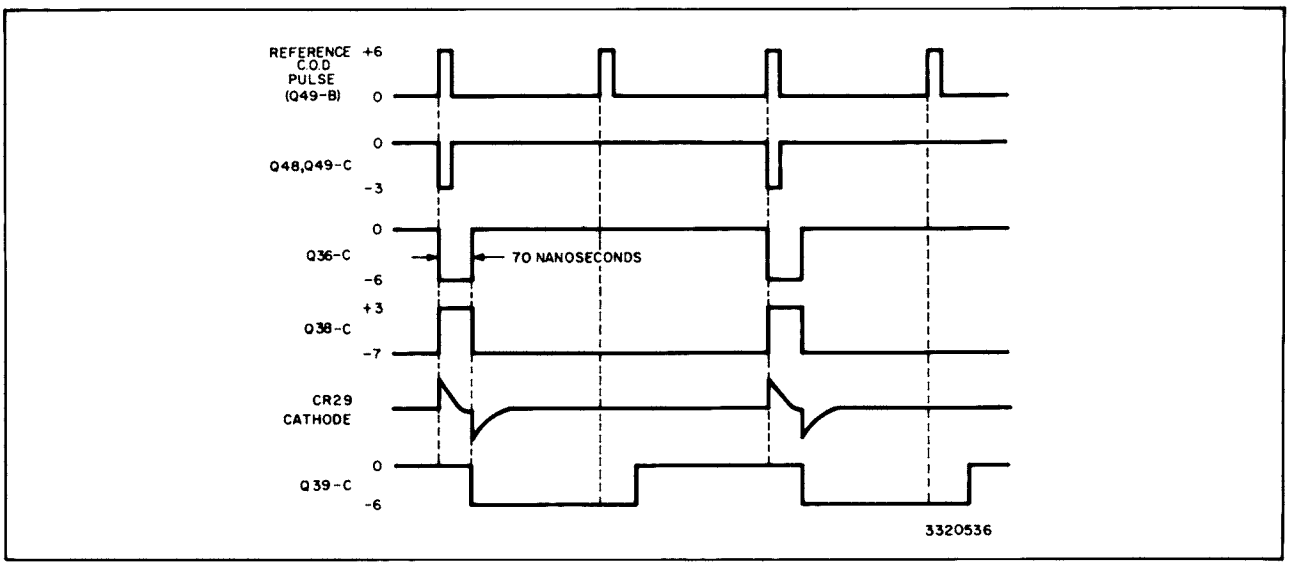


Figure 49—Reference Subcarrier Divider and Delay Waveforms

Q36 is biased into saturation by current withdrawn from its base by the −10 volt supply through resistors R115 and R116 and transistor Q37 is cut off by the contact potential of diode CR28 which is forward biased by the positive potential applied to its anode. The sharp positive-going edge of the triggering pulse from amplifier transistor Q47 is fed to the base of transistor Q36 via capacitor C48 and diode CR25 and drives the transistor into cut-off, thus beginning the multivibrator timed cycle (unstable state).

At the instant transistor Q36 is driven into cut-off its collector potential falls to approximately −6 volts. Simultaneously, capacitor C49 begins to charge toward −10 volts through resistors R112 and R113 since the initial current surge through resistor R113 results in a voltage drop which reverse-biases diode CR27. The current required by the charging action of capacitor C49 is drawn from the +70 volt supply via resistor R114 and from the base of transistor Q37. Current withdrawn from the base of transistor Q37 biases the transistor into saturation, and the emitter-to-base contact potential of Q37 (approximately −0.2 volt) reverse-biases diode CR28. As capacitor C49 charges toward −10 volts the current drawn from the +70 volt supply and the base of transistor Q37 decreases. When the total charging current has reached the value of the constant current supplied by the +70 volt supply via resistor R114, the current withdrawn from the base of transistor Q37 is zero and the transistor cuts off. A potential of approximately −3 volts then appears at the collector of transistor Q37, and this potential causes current to be withdrawn from the base of transistor Q36. Current withdrawn from the base of transistor Q36 biases the transistor into saturation once again and the multivibrator timed cycle ends. During the multivibrator timed cycle diode CR25 is reverse-biased by a positive potential applied to its cathode from the voltage divider network between +70 volts and ground consisting of resistor R110 and resistors R128 and R115 in parallel. Thus during the timed cycle the multivibrator is disconnected from the trigger amplifier circuit of transistor Q47, and noise or other spurious signals are thereby prevented from affecting the multivibrator timing circuit.

The duration of the multivibrator timed cycle is determined by the rate at which capacitor C49 charges through resistors R112 and R113 toward −10 volts. Due to the values of the components in the timing circuit and the amplitude of the charging current, the timed cycle is very short (approximately 70 nanoseconds). Therefore the signal at the collector of transistor Q37 (figure 48C) is a positive-going pulse which occurs at one-half the subcarrier rate and has a negative-going trailing edge delayed by approximately 70 nanoseconds with respect to the positive-going leading edge of the reference C.O.D. pulse. The pulse at the collector of transistor Q37 is fed to the burst divider circuit (described later) where the delayed edge is utilized in triggering a bistable multivibrator. Similarly, the signal at the collector of transistor Q36 is a 70 nanosecond pulse occurring at one-half the subcarrier rate (figures 48D and 48E). This pulse is negative-going however, and therefore it is the positive-going trailing edge which is delayed 70 nanoseconds with respect to the positive-going leading edge of the reference C.O.D. pulse. (See timing diagram, figure 49.)

During normal stable conditions, transistor Q36 in the reference delay multivibrator circuit is saturated and its collector is at ground potential. The divider network consisting of resistors R117 and R169 connected between −20 volts and ground then establishes a potential at the base of transistor Q38 which is positive with respect to −10 volts, and Q38 is thereby biased into saturation by current withdrawn from its base. When transistor Q38 is saturated its base potential is approximately −9.8 volts and diode CR16 is reverse-biased. The negative-going pulse at the collector of transistor Q36 forward biases diode CR16, thus driving the base of transistor Q38 negative with respect to its emitter by an amount equivalent to the contact potential of CR16 and the transistor is cut off. Transistor Q38 thus amplifies and inverts the negative-going 70 nanosecond reference delay multivibrator output pulse and inductor L16, utilized as a peaking coil, insures that the pulse at the collector of Q38 will have sharp edges.

The positive-going pulse at the collector of trigger amplifier transistor Q38 is fed to the monostable reference divider gate clamp multivibrator consisting of transistors Q39-Q40 and associated circuit components. In the multivibrator stable state, transistor Q39 is biased into saturation by current withdrawn from its base and transistor Q40 is biased into cut-off by a positive potential applied to its base from the divider network consisting of resistor R125 and resistors R124 and R121 in parallel. When transistor Q39 is saturated its base is at ground potential, and when transistor Q40 is cut off its collector is at approximately −10 volts. Therefore, during the multivibrator stable state the base potential of transistor Q39 is approximately 10 volts positive with respect to the collector of transistor Q40.

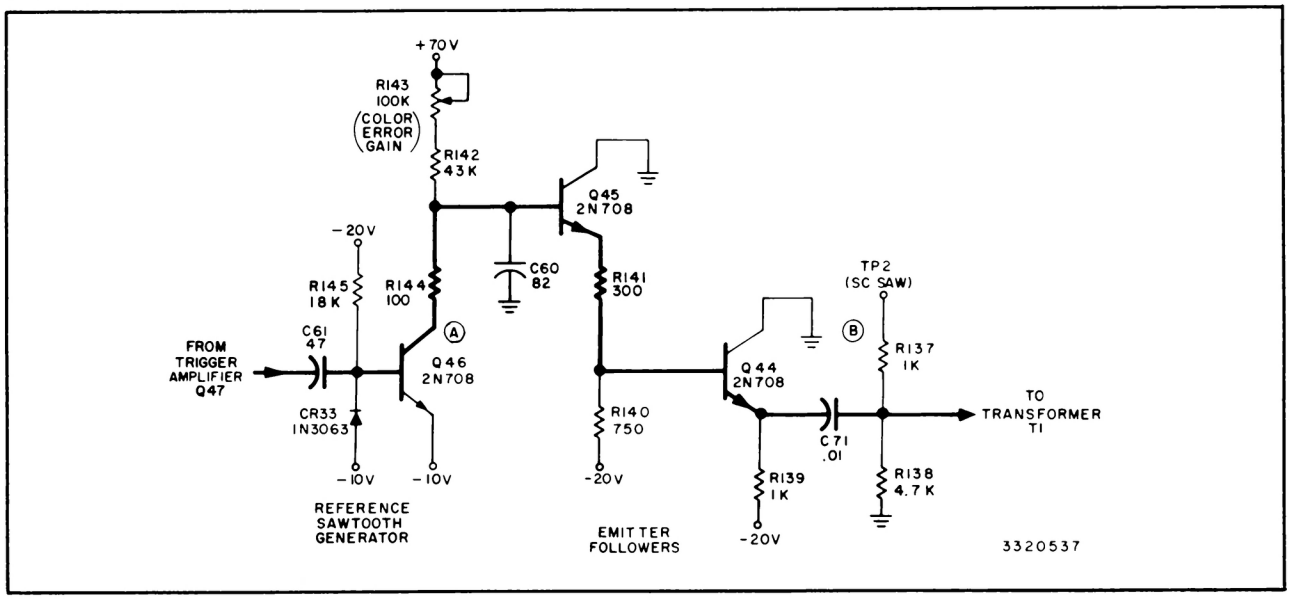
The positive-going pulse fed to the monostable multivibrator is differentiated by capacitor C52 and resistor R124, thus resulting in positive- and negative-going spikes which correspond to the leading and trailing edges respectively of the incoming pulse. The positive-going spike has no effect on the multivibrator action; however, the negative-going spike passes through diode CR29 to the base of transistor Q40 and drives Q40 into saturation. When transistor Q40 is driven into saturation its collector potential rises to ground. Since the potential across capacitor C51 cannot change instantaneously, the base potential of transistor Q39 remains 10 volts positive with respect to the collector potential of transistor Q40 and is thus approximately 10 volts positive with respect to ground. This potential biases transistor Q39 into cut-off and begins the multivibrator timed cycle (unstable state). As capacitor C51 discharges through resistor R119, the base potential of transistor Q39 falls toward −10 volts. When the base potential of transistor Q39 becomes slightly negative with respect to ground Q39 is biased into saturation once again and the timed cycle ends. During the multivibrator timed cycle diode CR29 is reverse-biased by the emitter-to-base contact potential of transistor Q40, thus disconnecting the multivibrator from the preceding trigger amplifier circuit and thereby isolating the multivibrator timing circuit from outside influence during the timed cycle.

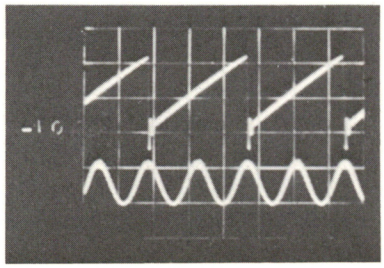
The duration of the multivibrator timed cycle is determined by the rate at which capacitor C51 discharges through resistor R119 toward −10 volts, and the component values are such that the timed interval is approximately 280 nanoseconds. Therefore the signal at the collector of transistor Q39 is an approximate square wave having a frequency equal to one-half the reference subcarrier frequency and thus one-half the incoming reference C.O.D. pulse frequency. The square wave is applied to the base of transistor Q48 in the reference divider 'AND' gate circuit (figures 48G and 48H), where it controls Q48 so that the transistor is cut off during the occurrence of every second reference C.O.D. pulse. Since the reference divider 'AND' gate circuit produces an output pulse only when a reference C.O.D. pulse is applied to transistor Q49 and transistor Q48 is simultaneously cut off, the desired frequency division by two is attained.

Reference Sawtooth Generator

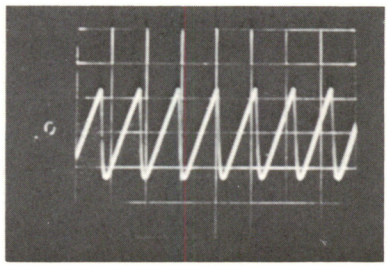
The sawtooth generator circuit shown in figure 50 develops a sawtooth waveform which occurs at one-half the reference subcarrier frequency and is timed to the leading edge of the reference C.O.D. (crossover detector) pulse. In the sawtooth generator circuit, transistor Q46 is normally biased into cut-off by the contact potential of diode CR33 which in turn is forward-biased by the negative potential applied to its cathode. The positive-going trigger pulse from trigger amplifier transistor Q47 drives transistor Q46 into saturation and the collector potential of Q46 is then approximately −9.6 volts.

When transistor Q46 is driven into saturation, capacitor C60 immediately discharges to approximately −9.6 volts. Since the pulse which triggers transistor Q46 is relatively narrow, Q46 is rapidly returned to its cut-off condition and capacitor C60 begins to charge through resistor R142 and potentiometer R143 toward +70 volts. The charging rate of capacitor C60 is determined by the values of C60 and resistor R142, in addition to the setting of potentiometer R143. The values of capacitor C60 and resistor R142 are such that even with potentiometer





A. Top: Q46 collector, 2v/cm.
Bottom: Reference SC (P1-21), 1v/cm.
ERROR GAIN maximum.
(0.2 μsec/cm)



B. TP2 (SC SAW), 1v/cm.
(0.5 μsec/cm)

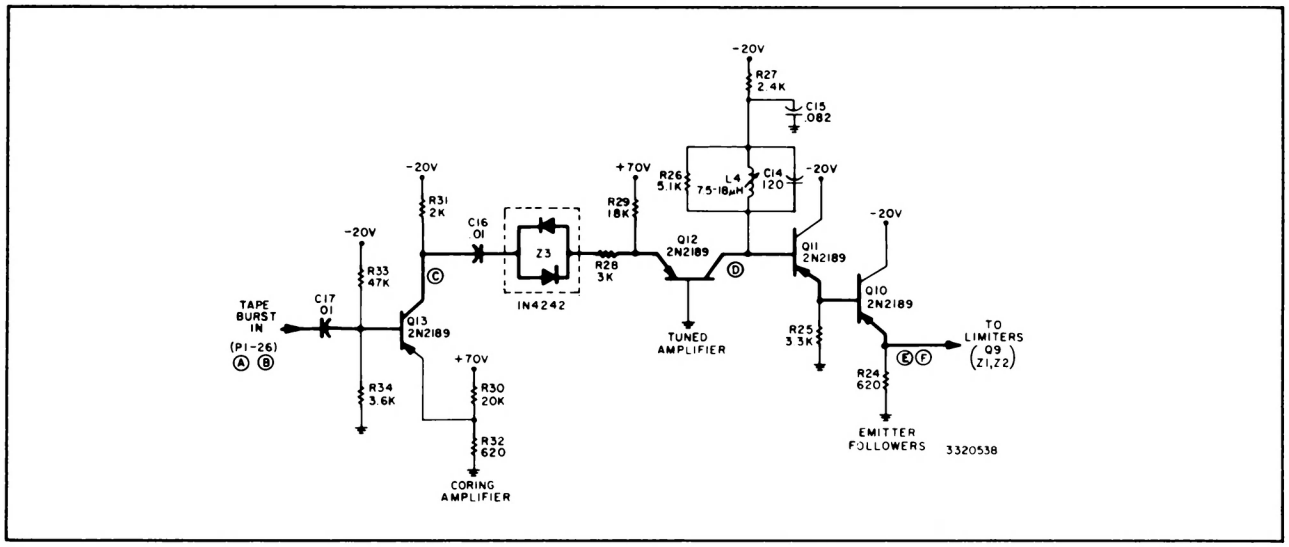
Machine in STOP mode (back-to-back signal).

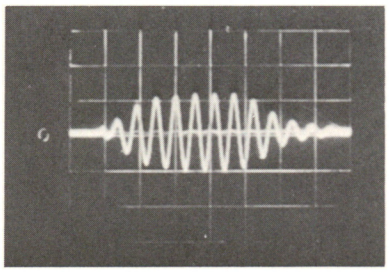
Figure 50—Reference Sawtooth Generator

R143 adjusted for minimum resistance the R142-C60 time constant is large when compared with the trigger pulse period; thus C60 will charge only several volts before transistor Q46 is driven into saturation by the next trigger pulse and C60 discharges once again.

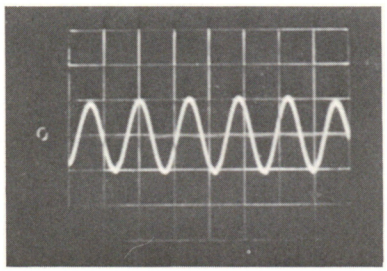
The resulting signal at the collector of transistor Q46 is a sawtooth waveform (figure 50A) which is timed to the leading edge of the reference C.O.D. pulse and has a slope determined by the charging rate of capacitor C60. Potentiometer R143 (COLOR ERROR GAIN) is provided as a means of varying the charging rate of capacitor C60, and thus the sawtooth waveform slope, over a small range. As potentiometer R143 is adjusted toward its maximum resistance position, the R142, R143-C60 time constant increases and thus the slope of the sawtooth waveform becomes flatter. The slope of the sawtooth waveform determines the error gain, and a procedure for adjusting potentiometer R143 to obtain the correct error gain is outlined under *Adjustments* at the end of the module circuit description.

Transistor Q45 functions as an emitter follower, and its purpose is to provide isolation between the sawtooth generator circuit and transformer T1. The sawtooth signal applied to the base of transistor Q45 also appears at its emitter, and the divider network consisting of resistors R140 and R141 reduces the amplitude of the signal applied to the base of transistor Q44 by approximately 30%. Transistor Q44 also functions as an emitter follower in providing additional isolation, and the sawtooth signal appearing at the emitter of Q44 is a-c coupled to transformer T1. Test point TP2 (SC SAW) is provided for convenience in observing the sawtooth signal fed to the transformer (figure 50B).

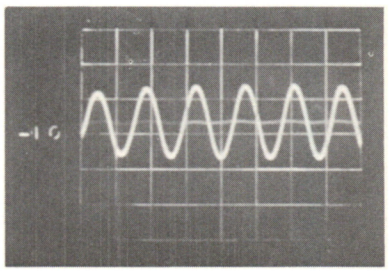




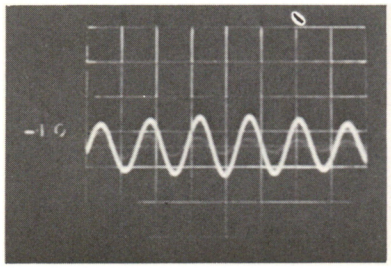
A. Tape burst (P1-26), 1v/cm. (0.5 μsec/cm)



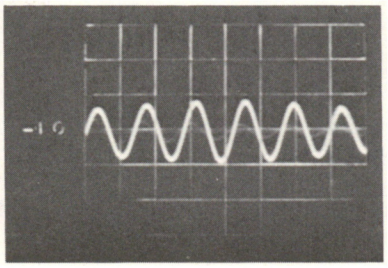
B. Tape burst (P1-26), 1v/cm.



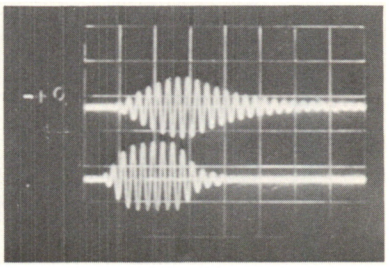
C. Q13 collector, 2v/cm.



D. Q12 collector, 2v/cm.



E. Q10 emitter, 2v/cm.



F. Top: Q10 emitter, 2v/cm. Bottom: Tape burst (P1-26), 1v/cm. (1 μsec/cm)

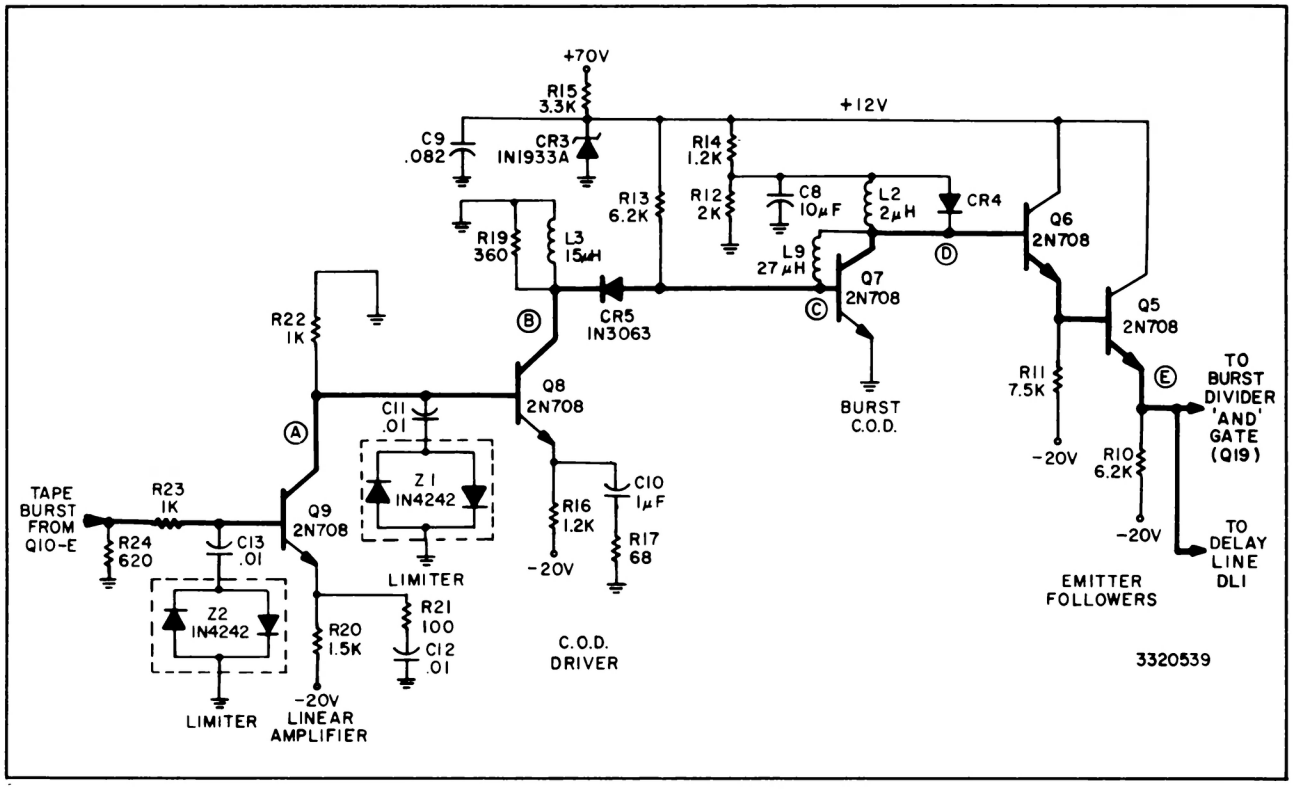
Machine in STOP mode (back-to-back signal). All sweep times 0.2 μsec/cm unless otherwise noted.

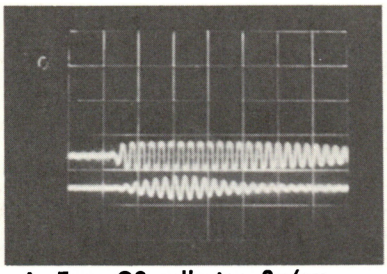
Figure 51—Burst Corer and Amplifier

Burst Corer and Amplifier

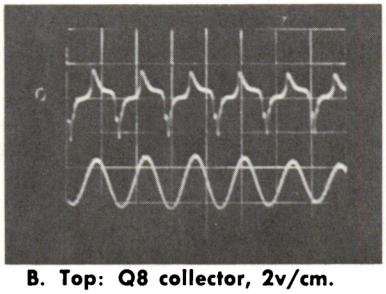
The function of the burst corer and amplifier circuit is to remove a small portion from the center of the tape burst signal so that noise or other spurious signals which may appear on the burst signal baseline will be eliminated. Burst is then restored to its original sinusoidal form by a parallel-tuned "ringing" circuit before being fed to limiters.

The tape burst signal fed to coring amplifier transistor Q13 via pin 26 of plug P1 (figure 51A) is obtained from the burst separator circuit in the chroma separator module and has an amplitude of approximately 2 volts peak-to-peak maximum, as shown in figure 51B. The voltage divider network consisting of resistors R33 and R34 establishes a bias potential of approximately −1.4 volts at the base of transistor Q13. This potential biases transistor Q13 into conduction, and the burst signal fed to its base is amplified by a ratio of approximately 3 to 1. The amplified burst signal appearing at the collector of transistor Q13 (figure 51C) is then a-c coupled to the coring network Z3.

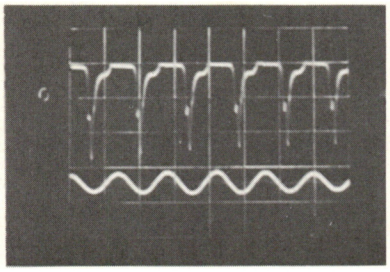




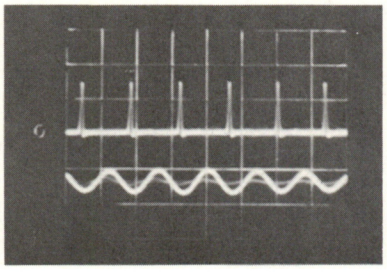
A. Top: Q9 collector, 2v/cm.
Bottom: Q10 emitter, 5v/cm.
(1 μsec/cm)



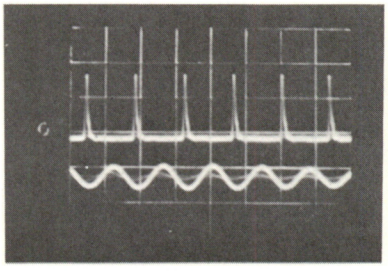
B. Top: Q8 collector, 2v/cm.
Bottom: Q10 emitter, 2v/cm.



C. Top: Q7 base, 1v/cm.
Bottom: Q10 emitter, 5v/cm.



D. Top: Q7 collector, 5v/cm.
Bottom: Q10 emitter, 5v/cm.



E. Top: Q5 emitter, 5v/cm.
Bottom: Q10 emitter, 5v/cm.

Machine in STOP mode (back-to-back signal). All sweep times 0.2 μsec/cm unless otherwise noted.

Figure 52—Tape Burst Limiters and Crossover Detector

Coring network Z3 consists of two unitized 1N4242 diodes, each having a contact potential of approximately 0.6 volt. Since the burst signal is a-c coupled to the coring network, only the portion of the burst signal having an amplitude which exceeds the diode contact potential in the positive or negative direction will forward bias the diodes and pass to the tuned amplifier circuit of transistor Q12. Thus the center portion of the burst signal, having an amplitude of approximately 1.2 volts, will be removed by the coring network.

Transistor Q12 functions as a common-base voltage amplifier, and is biased into conduction by current withdrawn from its base due to the positive potential applied to its emitter. Variable inductor L4, capacitor C14, and resistor R26 form a parallel circuit which is tuned to the subcarrier frequency. The parallel-tuned circuit removes harmonics introduced into the burst signal by the coring network, thereby restoring the burst signal to its original sinusoidal form. A "ringing" effect produced by the tuned circuit insures a pure (noise-free) burst signal, thus protecting against phase shifting of the burst crossover detector pulse which is derived from the burst signal as explained in the crossover detector circuit discussion below. Although the parallel-tuned circuit is tuned for resonance at the subcarrier frequency in general, its precise tuning is critical since the tuning has a definite effect on residual jitter. For this reason the procedure presented under *Adjustments* at the end of the module circuit description should be followed in tuning inductor L4.

The pure burst signal appearing at the collector of tuned amplifier transistor Q12 (figure 51D) is fed to emitter followers Q11 and Q10 in series. The emitter followers insure a constant loading on the tuned circuit and provide the current required to drive the limiter circuits which follow. Figures 51E and 51F show the burst signal at the emitter of transistor Q10.

Tape Burst Limiter and Crossover Detector

The function of the burst limiter and crossover detector circuit is to generate a positive-going pulse from the tape burst signal. The generated pulse has a sharp positive-going edge timed to the point at which the burst signal crosses the zero axis in a positive-going direction, and is designated the burst C.O.D. (crossover detector) pulse. The burst C.O.D. pulse is utilized in developing the phase sample pulse which will be discussed later.

The pure burst signal obtained from emitter follower transistor Q10 in the burst corer and tuned amplifier circuit is fed to the limiting circuit consisting of limiters Z2 and Z1 and linear amplifier transistor Q9 (figure 52). Limiters Z2 and Z1 are unitized matched pairs of 1N4242 diodes, with each diode having a contact potential of approximately 0.6 volt. Therefore, since capacitor C13 represents a low impedance at the burst frequency, all portions of the incoming burst signal which exceed 0.6 volt in either the positive or negative direction forward bias one or the other of the diodes of limiter Z2 and are thereby bypassed to ground. Thus the burst signal appearing at the base of amplifier transistor Q9 is limited in amplitude to approximately 1.2 volts peak-to-peak.

Transistor Q9 is biased into conduction by current withdrawn from its base due to the negative potential applied to its emitter, and the biasing arrangement is such that the limited burst signal will neither drive Q9 into saturation nor into cut-off. Transistor Q9 thus provides a linear gain and, due to its emitter and collector impedances, the gain is approximately 10 to 1. Limiter Z1, functioning exactly as does limiter Z2, further limits the signal appearing at the collector of transistor Q9 so that the signal applied to the base of transistor Q8 approaches a square wave with an amplitude of approximately 1.2 volts peak-to-peak and a sharp positive-going edge (figure 52A).

Transistor Q8 functions as the crossover detector driver, and a d-c potential of approximately −5 volts applied to its base causes a base current to flow which biases the transistor into conduction. The square wave signal fed to the base of transistor Q8 is differentiated by the parallel combination of resistor R19 and inductor L3 in the collector circuit of Q8. The differentiation network has the effect of amplifying the high frequency components (sharp edges) of the signal fed to transistor Q8, whereas inductor L3 provides a low impedance path to ground for the lower frequency signal components. Therefore, due to a polarity inversion and the differentiation action, the signal at the collector of transistor Q8 has a sharp negative-going edge and an amplitude of approximately 4 volts peak-to-peak as shown in figure 52B.

Burst crossover detector (C.O.D.) transistor Q7 is normally biased into conduction by current supplied to its base via resistor R13; therefore the base of Q7, and thus the anode of diode CR5, is normally at ground potential. The positive-going portion of the signal at the collector of transistor Q8 reverse-biases diode CR5 and therefore does not appear at

the base of transistor Q7. However the sharp negative-going edge of the signal forward biases diode CR5 and thereby drives transistor Q7 into cut-off. Inductor L9 prevents transistor Q7 from saturating when the transistor is biased into conduction, while at the same time provides sufficient impedance to develop the sharp pulse required to cut Q7 off.

During the interval that burst crossover detector transistor Q7 is conducting, its collector is at ground potential. When transistor Q7 is driven into cut-off by the negative-going edge of the signal fed to its base, its collector voltage rises toward a potential of approximately +7.5 volts established by the divider network consisting of resistors R14 and R12 connected between +12 volts and ground, but is prevented from reaching this level by the action of inductor L2. Inductor L2 would normally have a "ringing" effect in the collector circuit of transistor Q7; however, after the positive-going half-cycle of the waveform occurs, the negative-going half-cycle forward biases diode CR4, thus bypassing the inductor, and the remainder of the waveform is effectively damped out. Therefore, due to the action of inductor L2 and diode CR4, the signal at the collector of transistor Q7 is a positive-going pulse which occurs at the burst frequency and has an amplitude of approximately 7 volts as shown in figure 52D.

The high frequency peaking action of inductor L2 insures that the burst C.O.D. output pulse will have a rapid positive-going (leading) edge, and it is this edge which bears a definite phase relationship to the burst crossover point (i.e., the point at which the tape burst sine wave crosses the zero axis in a positive-going direction). Therefore, regardless of the amount that the tape burst signal may be shifted in phase, the *difference* in phase between the burst crossover point and the rapid positive-going edge of the pulse at the collector of transistor Q7 will remain constant. Emitter follower transistors Q6 and Q5 in series provide the current gain required to drive transistor Q19 in the burst divider 'AND' gate and delay line DL1. Figure 52E shows the positive-going burst C.O.D. pulse which appears at the emitter of emitter follower transistor Q5.

The +12 volt potential utilized in the burst C.O.D. circuit is obtained from the network which includes resistor R15, capacitor C9, and Zener diode CR3. Zener diode CR3 is reverse-biased by the positive potential applied to its cathode, thus causing the diode breakdown voltage (characteristically +12 volts) to appear at the junction of CR3 and resistor R15. Resistor R15 is utilized as a current limiting resistor, and capacitor C9 provides a low impedance bypass to ground for the higher frequency signal components.

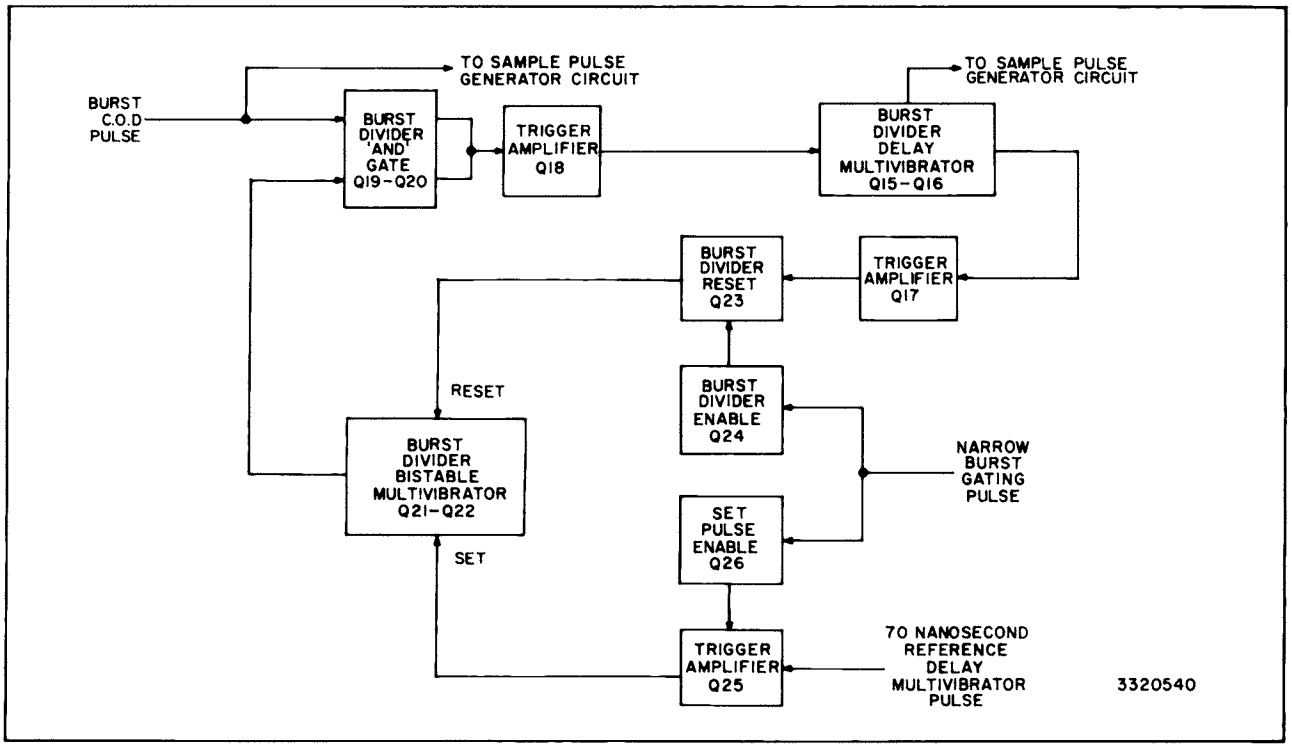


Figure 53—Tape Burst Divider and Delay Block Diagram

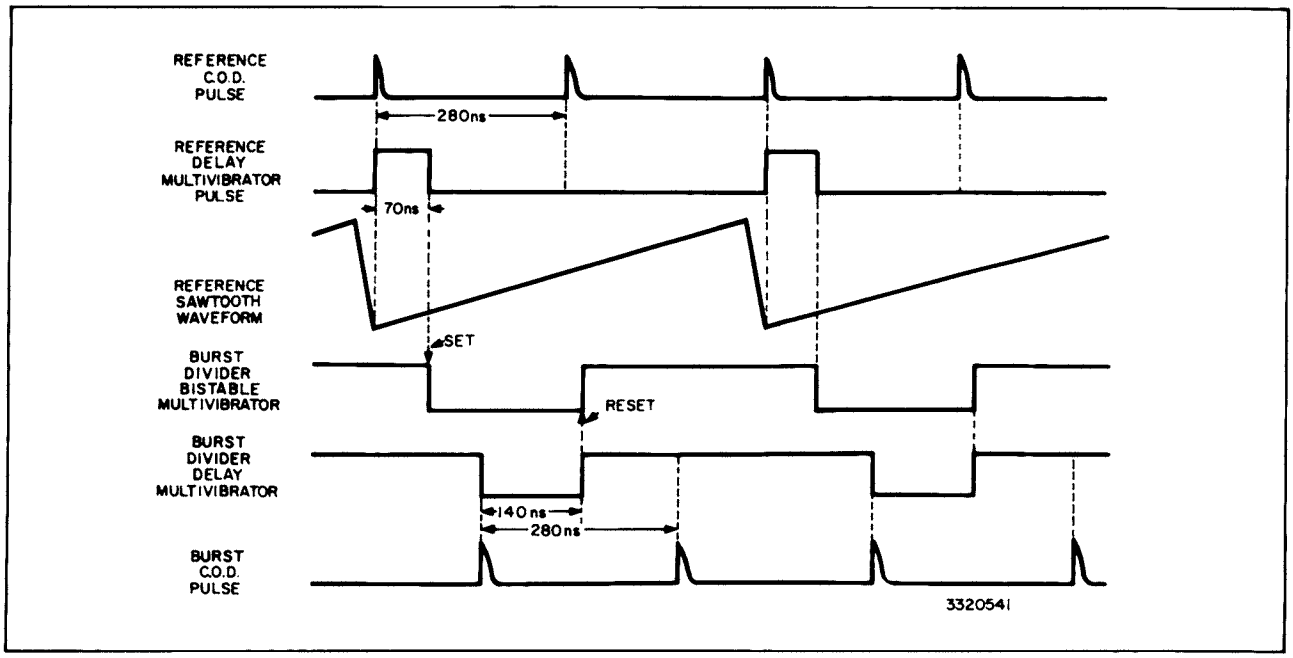


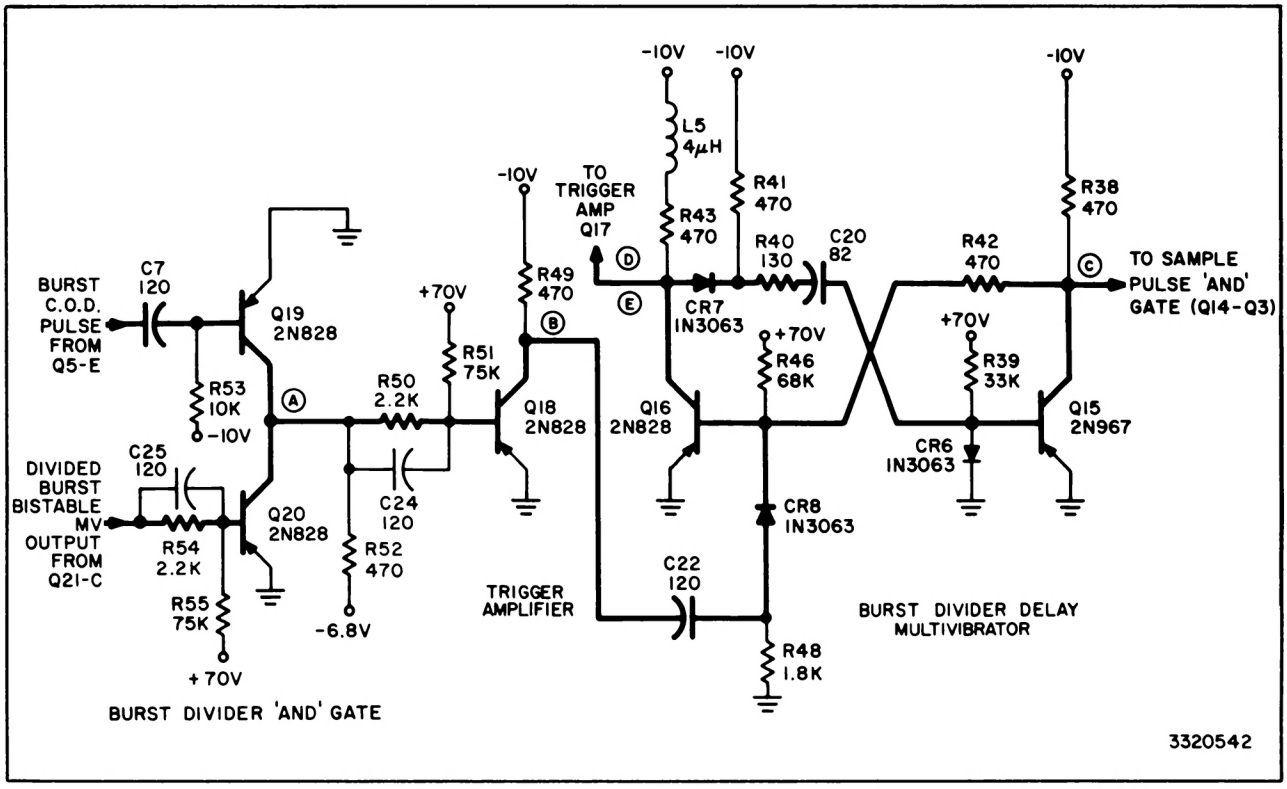
Figure 54—Tape Burst Divider and Delay Circuit Timing Diagram

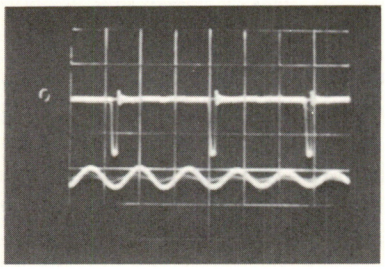
Tape Burst Divider and Delay Circuit

The tape burst divider and delay circuit is shown in block diagram form in figure 53. The purpose of this circuit is to produce a pulse which occurs at one-half the tape burst frequency and has a leading edge timed to the leading edge of the burst C.O.D. pulse and a trailing edge delayed by 140 nanoseconds with respect to the leading edge of the burst C.O.D. pulse. The resulting 140 nanosecond output pulse is utilized in conjunction with the burst C.O.D. pulse in generating the phase sample pulse.

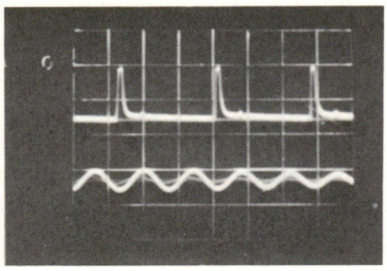
The heart of the tape burst divider and delay circuit is the burst divider bistable multivibrator. The bistable multivibrator is "set" by a pulse derived from the trailing edge of the output pulse from the reference delay multivibrator. The reference delay multivibrator output pulse occurs at one-half the reference subcarrier rate and has a leading edge timed to the reference C.O.D. pulse and a trailing edge delayed by 70 nanoseconds with respect to the leading edge of the reference C.O.D. pulse. Since the beginning of the reference sawtooth waveform slope is also timed to the leading edge of the reference C.O.D. pulse, the bistable multivibrator is set approximately 70 nanoseconds after the beginning of each reference sawtooth slope. (See *Tape Burst Divider and Delay Circuit Timing Diagram,* figure 54.) Once set, the bistable multivibrator is re-set by a pulse derived from the burst divider multivibrator output. Both the set and reset pulses are controlled by the narrow burst gating pulse in such a manner that the tape burst divider and delay circuit will function only during the narrow burst gating pulse interval.

The bistable multivibrator output is fed to an 'AND' gate which also receives the burst C.O.D. pulse. The 'AND' gate may be opened only when the bistable multivibrator is "set"; therefore the first burst C.O.D. pulse to appear at the 'AND' gate after the bistable multivibrator has been set opens the gate and produces a pulse. Since the bistable multivibrator receives a set pulse at one-half the reference subcarrier rate, and is re-set before the second consecutive burst C.O.D. pulse is applied to the 'AND' gate, the 'AND' gate output pulse occurs at one-half the subcarrier (or tape burst) frequency. The 'AND' gate output pulse triggers the burst divider delay multivibrator, which in turn produces an output pulse at one-half the tape burst rate. The leading edge of the burst divider delay multivibrator output pulse is timed to the leading edge of the burst C.O.D. pulse, and the trailing edge of the pulse is delayed by 140 nanoseconds with respect to the leading edge of the burst C.O.D. pulse. The trailing (delayed) edge of the delay multivibrator output pulse is utilized in generating the bistable multivibrator reset pulse; thus the bistable multivibrator is re-set 140 nanoseconds after the 'AND' gate has produced an output pulse and the desired divide-by-two action is attained. (Refer to the timing diagram, figure 54.)

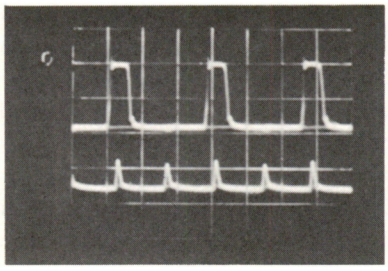




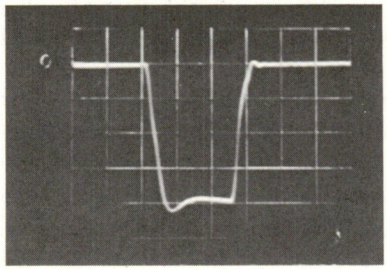
A. Top: Q19 collector, 2v/cm.
Bottom: Q10 emitter, 5v/cm.



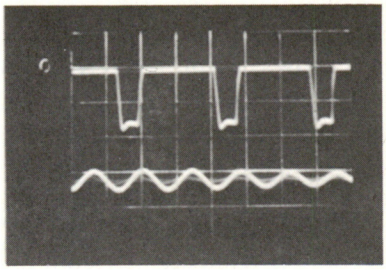
B. Top: Q18 collector, 5v/cm.
Bottom: Q10 emitter, 5v/cm.



C. Top: Q15 collector, 2v/cm.
Bottom: Q4 collector, 5v/cm.



D. Q16 collector, 2v/cm.
(.05 μsec/cm)



E. Top: Q16 collector, 5v/cm.
Bottom: Q10 emitter, 5v/cm.

Machine in STOP mode (back-to-back signal). All sweep times 0.2 μsec/cm unless otherwise noted.

Figure 55—Burst Divider 'AND' Gate and Delay Multivibrator Circuits

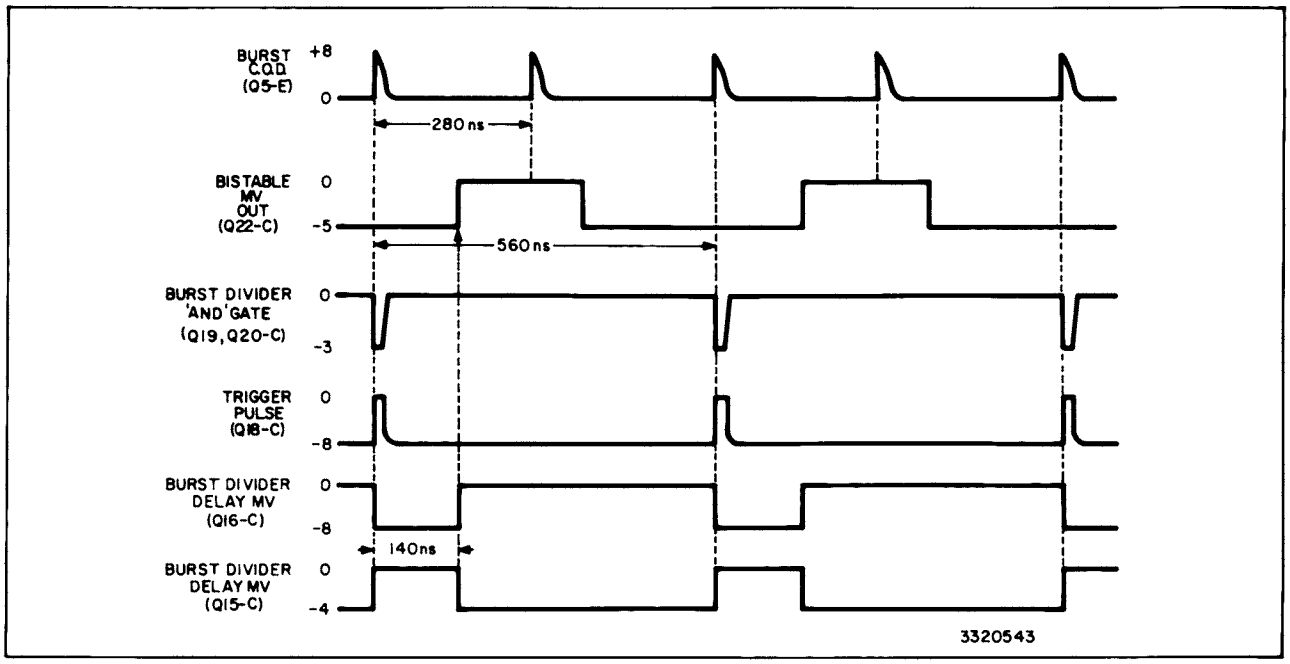


Figure 56—Burst Divider 'AND' Gate and Delay Multivibrator Waveforms

A. Burst Divider 'AND' Gate and Delay Multivibrator

The burst divider 'AND' gate consists of transistors Q19-Q20 and associated circuit components, as shown in figure 55. Since the collectors of transistors Q19 and Q20 are common, the potential at the common collector is dependent upon the state of each transistor. When either transistor is saturated, the common collector is at ground potential; when both transistors are simultaneously in the cut-off state, the common collector potential falls to some negative value.

The 'AND' gate is controlled by a rectangular waveform fed to the base of transistor Q20 from the collector of transistor Q21 in the divided burst bistable multivibrator circuit. The development of the rectangular waveform will be explained later during the bistable multivibrator circuit discussion, and it is sufficient to state here that the waveform occurs at one-half the burst frequency and has a positive-going edge which is delayed by 140 nanoseconds with respect to the positive-going (leading) edge of the burst C.O.D. pulse. (See timing diagram, figure 56.) The potential at the collector of bistable multivibrator transistor Q21 is either ground or −5 volts, depending upon the multivibrator state. During the interval that the collector potential of transistor Q21 is −5 volts, the voltage distribution in the divider network consisting of resistors R54 and R55 is such that transistor Q20 is biased into saturation by current withdrawn from its base. The common collector of transistors Q19-Q20 is thereby clamped at ground potential, thus maintaining the 'AND' gate closed. When the collector potential of transistor Q21 rises to ground, the potential applied to the base of transistor Q20 from the voltage divider network is approximately +2 volts. This potential biases transistor Q20 into cut-off, thus permitting the 'AND' gate to open when a burst C.O.D. pulse appears at the base of transistor Q19.

The burst C.O.D. pulse fed to the base of transistor Q19 is positive-going and occurs at the burst frequency. Transistor Q19, normally biased into saturation by current withdrawn from its base, is driven into cut-off by the positive-going incoming pulse. When the 'AND' gate is opened by the rectangular waveform from the burst divider bistable multivibrator, the positive-going pulse which cuts off transistor Q19 causes the common collector potential of transistors Q19-Q20 to fall to some negative value. The resulting signal at the common collector of transistors Q19-Q20 is a negative-going pulse (figure 55A) having a leading edge which is timed to the positive-going leading edge of the burst C.O.D. pulse. Since the 'AND' gate is opened at a rate equal to one-half the burst frequency and the burst C.O.D. pulse occurs at the burst frequency, every second burst C.O.D. pulse will result in a negative-going output pulse from the 'AND' gate. (See timing diagram, figure 56.)

During the interval between negative-going 'AND' gate pulses the common collector of transistors Q19-Q20 is at ground potential, thus establishing a voltage divider network consisting of resistors R50 and R51 between +70 volts and ground. A potential of approximately +2 volts is applied to the base of trigger amplifier transistor Q18 from the divider, and this potential biases Q18 into cut-off. When both 'AND' gate transistors are cut off, the positive bias potential is removed from the base of transistor Q18 and the divider network consisting of resistors R52, R50, and R51 provides a negative potential which causes Q18 to become biased into saturation by current withdrawn from its base. When transistor Q18 is saturated its base is at ground potential and the amplitude of the negative-going 'AND' gate pulse is then approximately 3 volts as determined by the divider network consisting of resistor R52 and resistor R50 in parallel with capacitor C24, connected between ground and −6.8 volts.

Transistor Q18 amplifies the 'AND' gate pulse, and the resulting pulse at the collector of Q18 has an amplitude of approximately 8 volts (figure 55B) and a positive-going leading edge which is timed to the leading edge of the burst C.O.D. pulse. The output pulse at the collector of transistor Q18 is fed via diode CR8 to the base of transistor Q16 in the burst divider delay multivibrator circuit.

Transistors Q15-Q16 and associated circuit components form the monostable burst delay multivibrator. In the multivibrator stable state, transistor Q16 is biased into saturation by current withdrawn from its base by the −10 volt supply through resistors R42 and R38, and transistor Q15 is biased into cut-off by the contact potential of diode CR6 which is forward biased by the positive potential applied to its anode. The positive-going spike fed to the base of transistor Q16 drives Q16 into cut-off, thus beginning the multivibrator timed cycle (unstable state).

At the instant transistor Q16 is driven into cut-off its collector potential falls to approximately −8 volts. Simultaneously, capacitor C20 begins to charge toward −10 volts through resistors R40 and R41 since the initial current surge through resistor R40 results in a voltage drop which reverse-biases diode CR7 and thereby cuts the diode off. The current required by the charging action of capacitor C20 is drawn from the +70 volt supply via resistor R39 and from the base of transistor Q15. Current withdrawn from the base of transistor Q15 biases Q15 into saturation, and the emitter-to-base contact potential of Q15 (approximately −0.2 volt) reverse-biases diode CR6. As capacitor C20 charges toward −10 volts the total current drawn by the capacitor decreases. Due to the value of resistor R39 (33 K ohms) the +70 volt supply furnishes an essentially constant current, therefore the current drawn from the base of transistor Q15 must decrease. When the total charging current has decreased to the value of the constant current supplied by the +70 volt supply, the current withdrawn from the base of transistor Q15 is zero and the transistor is cut off. A potential of approximately −4 volts then appears at the collector of transistor Q15, and this potential causes current to be withdrawn from the base of transistor Q16. Current withdrawn from the base of transistor Q16 biases the transistor into saturation once again and the multivibrator timed cycle ends. During the multivibrator timed cycle, diode CR8 is reverse-biased by a positive potential applied to its cathode from the voltage divider network consisting of resistors R42 and R46 connected between ground potential at the collector of transistor Q15 and the +70 volt supply. Thus during the timed cycle the multivibrator is disconnected from the trigger amplifier circuit of transistor Q18, and noise or other spurious signals are thereby prevented from affecting the multivibrator timing circuit.

The duration of the multivibrator timed cycle is determined by the rate at which capacitor C20 charges through resistors R40 and R41 toward −10 volts. Due to the values of the components in the multivibrator timing circuit and the amplitude of the charging current, the timed cycle is comparatively short (approximately 140 nanoseconds). The signal at the collector of transistor Q15 (figure 55C) is thus a positive-going pulse which occurs at one-half the burst frequency and has a negative-going trailing edge delayed by approximately 140 nanoseconds with respect to the positive-going leading edge of the burst C.O.D. pulse. (See timing diagram, figure 56.) The positive-going pulse is fed to transistor Q14 in the sample pulse 'AND' gate circuit which is discussed in detail later.

Similarly, the signal at the collector of transistor Q16 is a 140 nanosecond pulse (figure 55D) occurring at one-half the burst frequency (figure 55E). This pulse is negative-going however, and therefore it is the positive-going trailing edge which is delayed 140 nanoseconds with respect to the positive-going leading edge of the burst C.O.D. pulse (figure 56). The negative-going pulse appearing at the collector of transistor Q16 is formed into the burst divider reset pulse which allows the burst divider bistable multivibrator to be triggered when other required conditions are met, as explained below.

B. Burst Divider Bistable Multivibrator

The purpose of the burst divider bistable multivibrator circuit is to produce a rectangular waveform occurring at one-half the burst frequency and having positive- and negative-going edges which bear fixed phase relationships to the reference and burst C.O.D. pulses respectively. Thus as the tape burst and reference subcarrier sinusoidal signals vary in relative phase, the widths of the rectangular waveform alternations vary accordingly. The bistable multivibrator is enabled only during the 2.5 microsecond narrow burst gating pulse interval; therefore approximately five cycles of the rectangular waveform occur during each TV line. Figure 57 shows the circuitry which develops the bistable set and reset pulses, as well as the narrow burst gate pulse enabling circuitry.

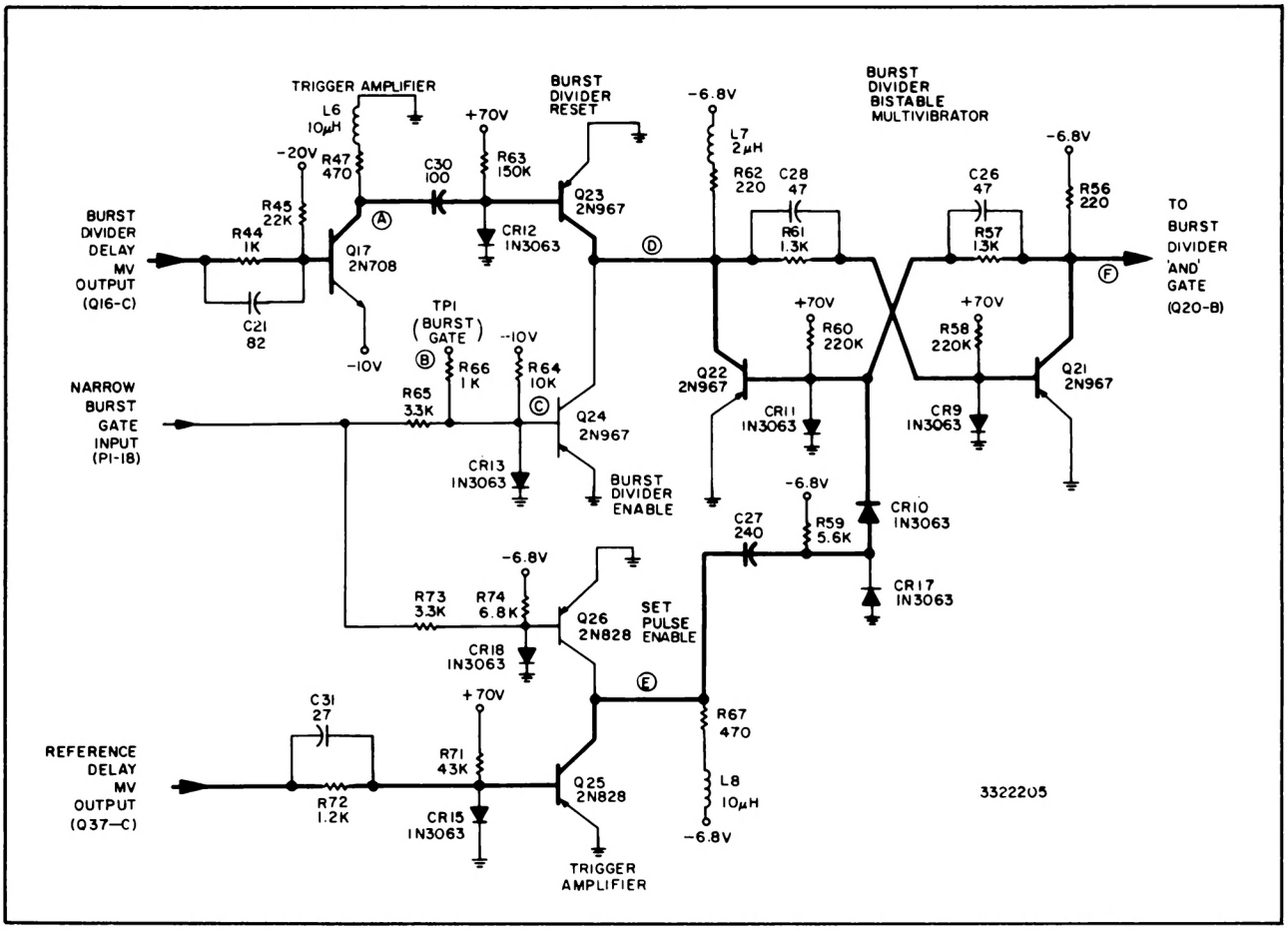
The bias potential applied to the base of trigger amplifier transistor Q17 is established by the voltage divider network consisting of resistors R44 and R45 connected between the −20 volt bus and the potential at the collector of transistor Q16 in the burst divider delay multivibrator circuit. The potential at the collector of transistor Q16 is ground during the delay multivibrator stable state and −8 volts during the 140 nanosecond unstable state, as explained in the delay multivibrator circuit discussion above and as shown on the timing diagram (figure 58). During the interval that the collector potential of transistor Q16 is ground, the negative potential appearing at the junction of voltage divider resistors R44 and R45 is actually positive with respect to the emitter potential of transistor Q17. Transistor Q17 is thereby biased into saturation by current withdrawn from its base, and its collector potential is approximately −8 volts. The negative-going leading edge of the 140 nanosecond pulse at the collector of transistor Q16 drives transistor Q17 into cut-off and the collector potential of Q17 rises to ground. The positive-going trailing edge of the 140 nanosecond pulse then drives transistor Q17 into saturation once again and, aided by the action of inductor L6, the collector potential of Q17 falls rapidly to −8 volts. The resulting output signal at the collector of transistor Q17 is a positive-going pulse having an amplitude of approximately 8 volts (figure 57A) and a rapid negative-going trailing edge which is timed to the trailing (delayed) edge of the output from transistor Q16 in the burst divider delay multivibrator circuit.

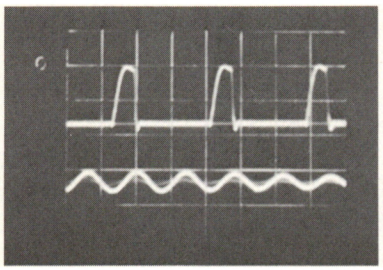
The positive-going pulse appearing at the collector of transistor Q17 is differentiated by the network consisting of capacitor C30 and resistor R63, and the resulting signal is fed to the base of burst divider reset transistor Q23. Transistor Q23 is normally cut off by the contact potential of diode CR12, which in turn is forward biased by the positive potential applied to its anode. The positive-going portion of the differentiated signal fed to the base of transistor Q23 has no effect on the transistor operation, however the negative-going spike, corresponding to the rapid negative-going edge of the pulse at the collector of transistor Q17, drives Q23 into saturation. Since the collectors of transistors Q22, Q23, and Q24 are common, the common collector potential is determined by the simultaneous state of all three transistors. As explained below, burst divider enable transistor Q24 is cut off only during the narrow burst gating pulse interval; therefore, during this interval the common collector potential is determined by the state of transistors Q22 and Q23.

The narrow burst gating pulse which controls burst divider enable transistor Q24 is developed in the chroma separator module, and may be observed at test point TP1. (See figure 57B.) During the interval between narrow burst gating pulses, current withdrawn from the base of transistor Q24 by the −10 volt supply via resistor R64 biases Q24 into saturation. The positive-going narrow burst gating pulse then forward biases diode CR13, and transistor Q24 is biased into cut-off by the contact potential of CR13 during the gating pulse interval (figure 57C).

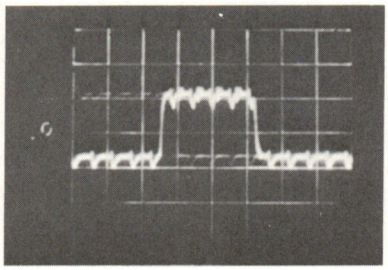
The burst divider bistable multivibrator has been established in its reset state (i.e., transistor Q22 saturated; transistor Q21 cut off), since ground potential provided by transistor Q24 when Q24 is saturated (between narrow burst gating pulses) will hold transistor Q21 in cut-off. When the narrow burst gating pulse drives transistor Q24 into cut-off the bistable multivibrator will remain in its reset state, regardless of the state of transistor Q23, until the multivibrator is "set" by a pulse from transistor Q25. Once the bistable multivibrator has been set (i.e., transistor Q21 saturated; transistor Q22 cut off), the next pulse from transistor Q17 will drive transistor Q23 into saturation and Q23 will provide the pulse which returns the multivibrator to its reset state. (See timing diagram, figure 58.)

The development of the burst divider bistable multivibrator set pulse is controlled by both the narrow burst gating pulse and the output from transistor Q37 in the reference delay multivibrator circuit. The output at the collector of transistor Q37

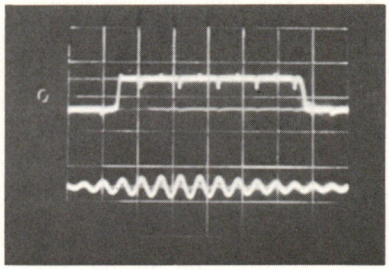




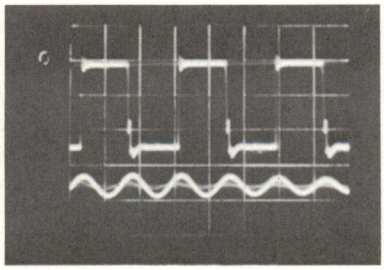
A. Top: Q17 collector, 5v/cm. Bottom: Q10 emitter, 5v/cm.



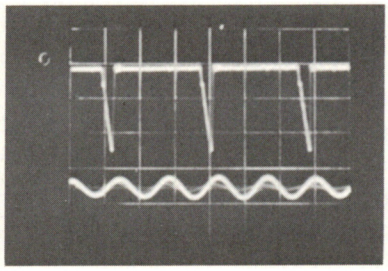
B. TP1 (BURST GATE), 0.5v/cm. (1 μsec/cm)



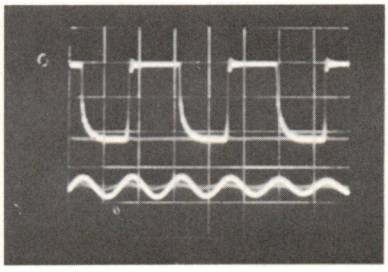
C. Top: Q24 base, 1v/cm. Bottom: Q10 emitter, 5v/cm. (0.5 μsec/cm)



D. Top: Q23 collector, 2v/cm. Bottom: Q10 emitter, 5v/cm.



E. Top: Q25 collector, 1v/cm. Bottom: Q10 emitter, 5v/cm.



F. Top: Q21 collector, 2v/cm. Bottom: Q10 emitter, 5v/cm.

Machine in STOP mode (back-to-back signal). All sweep times 0.2 μsec/cm unless otherwise noted.

Figure 57—Burst Divider Bistable Multivibrator Circuit

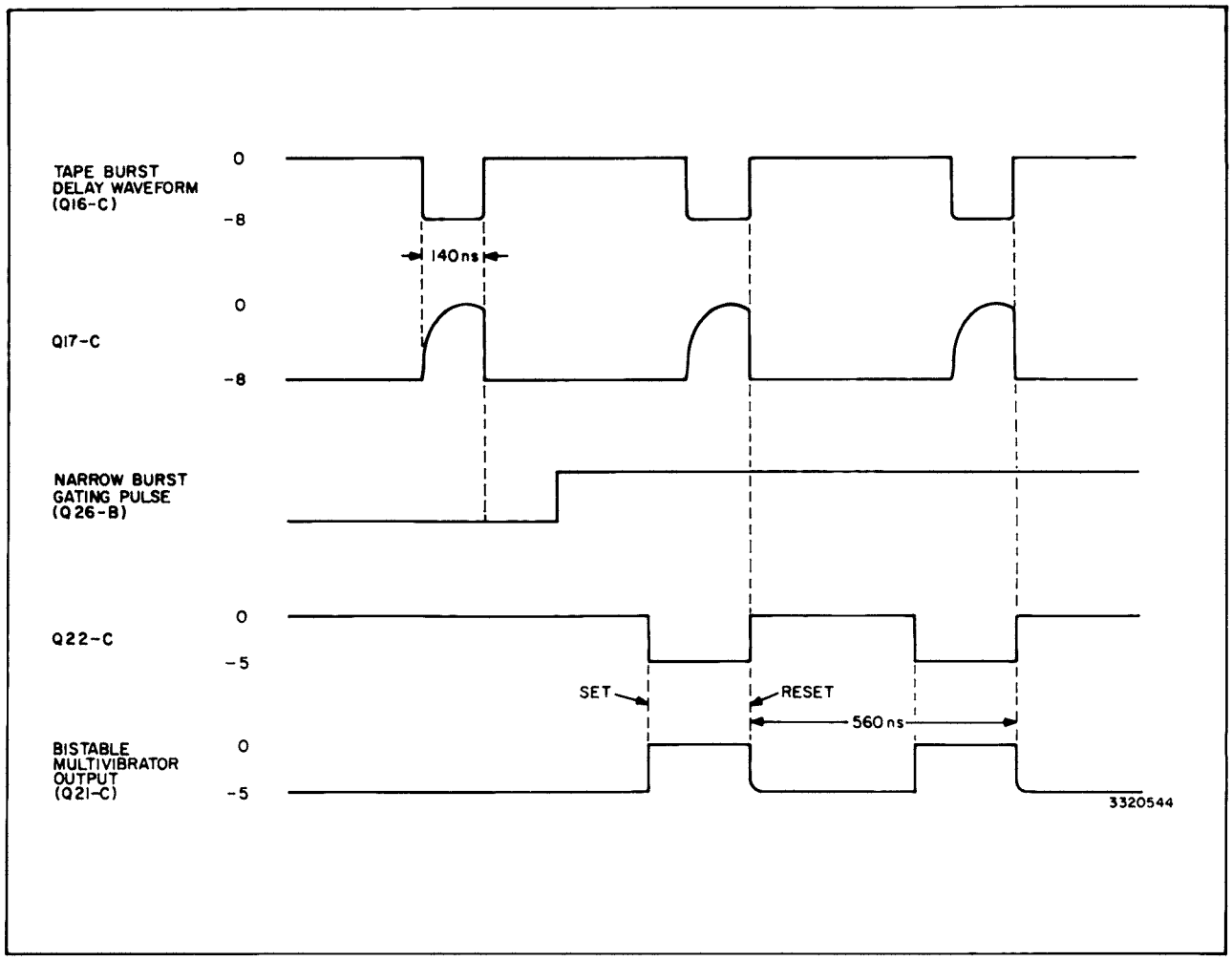


Figure 58—Burst Divider Bistable Multivibrator Reset Pulse Development

is a 70 nanosecond pulse which occurs at one-half the reference subcarrier rate and has a positive-going leading edge timed to the positive-going leading edge of the reference C.O.D. pulse. During the interval between 70 nanosecond pulses the collector potential of transistor Q37 is approximately −3 volts, and current withdrawn from the base of transistor Q25 by the negative potential biases Q25 into saturation. During the 70 nanosecond pulse interval the collector of transistor Q37 is at ground potential, and the resulting positive potential applied to the anode of diode CR15 from the divider network consisting of resistors R71 and R72 forward biases the diode. Transistor Q25 is then cut off by the contact potential of diode CR15, and the transistor remains cut off for the duration of the 70 nanosecond pulse.

The narrow burst gating pulse fed to burst divider enable transistor Q24 is also fed to set pulse enable transistor Q26. During the interval between narrow burst gating pulses, current withdrawn from the base of transistor Q26 by the −6.8 volt potential via resistor R74 biases the transistor into saturation. The positive-going narrow burst gating pulse then forward biases diode CR18, and transistor Q26 is biased into cut-off by the contact potential of CR18 for the duration of the narrow burst pulse.

Since the collectors of transistors Q25 and Q26 are common, the common collector potential is dependent upon the simultaneous state of each transistor. As mentioned above, during the narrow burst interval transistor Q26 is cut off and transistor Q25 is normally saturated. Therefore, during the narrow burst interval the common collector potential is ground until transistor Q25 is driven into cut-off by the positive-going edge of the 70 nanosecond pulse fed to its base and the common collector potential falls to −3 volts. The negative-going edge

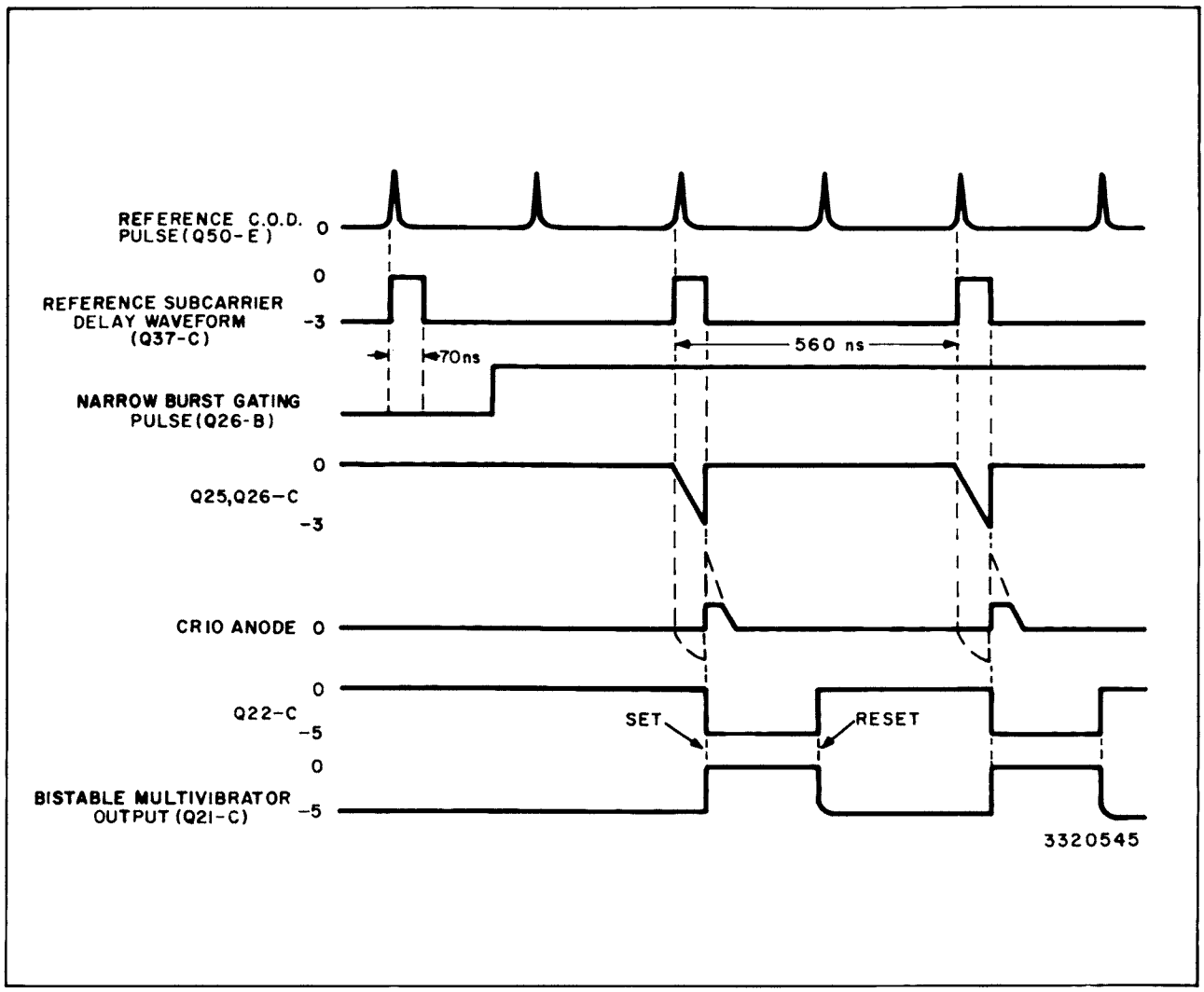


Figure 59—Burst Divider Bistable Multivibrator Set Pulse Development

of the 70 nanosecond pulse then drives transistor Q25 into saturation once again, and the result is a negative-going pulse at the common collector of transistors Q25-Q26 as shown in figure 57E. Due to the action of inductor L8 the pulse at the common collector has a very rapid positive-going edge, and this edge is timed to the trailing (delayed) edge of the output from transistor Q37 in the reference delay multivibrator circuit. (See timing diagram, figure 59.)

Capacitor C27 and resistor R59 form a network which differentiates the negative-going pulse output at the common collector of transistors Q25-Q26. The negative-going portion of the differentiated pulse is bypassed to ground by diode CR17 which is forward biased by the −6.8 volt potential applied to its cathode via resistor R59. The positive-going spike resulting from the differentiation corresponds to the rapid positive-going edge of the pulse at the common collector of transistors Q25-Q26. This spike reverse biases diode CR17 and forward biases diode CR10, and thus appears at the base of bistable multivibrator transistor Q22 as a triggering, or set, pulse.

Assuming transistor Q22 to be saturated, the collector of Q22 is at ground potential and transistor Q21 is biased into cut-off by the contact potential of diode CR9 which in turn is forward biased by the positive potential applied to its anode from the voltage divider network consisting of resistors R58 and R61 connected between the +70 volt supply and ground. The positive-going set pulse applied to the base of transistor Q22 drives Q22 into cut-off and thus removes the ground potential at its collector. Transistor Q21 is then biased into saturation

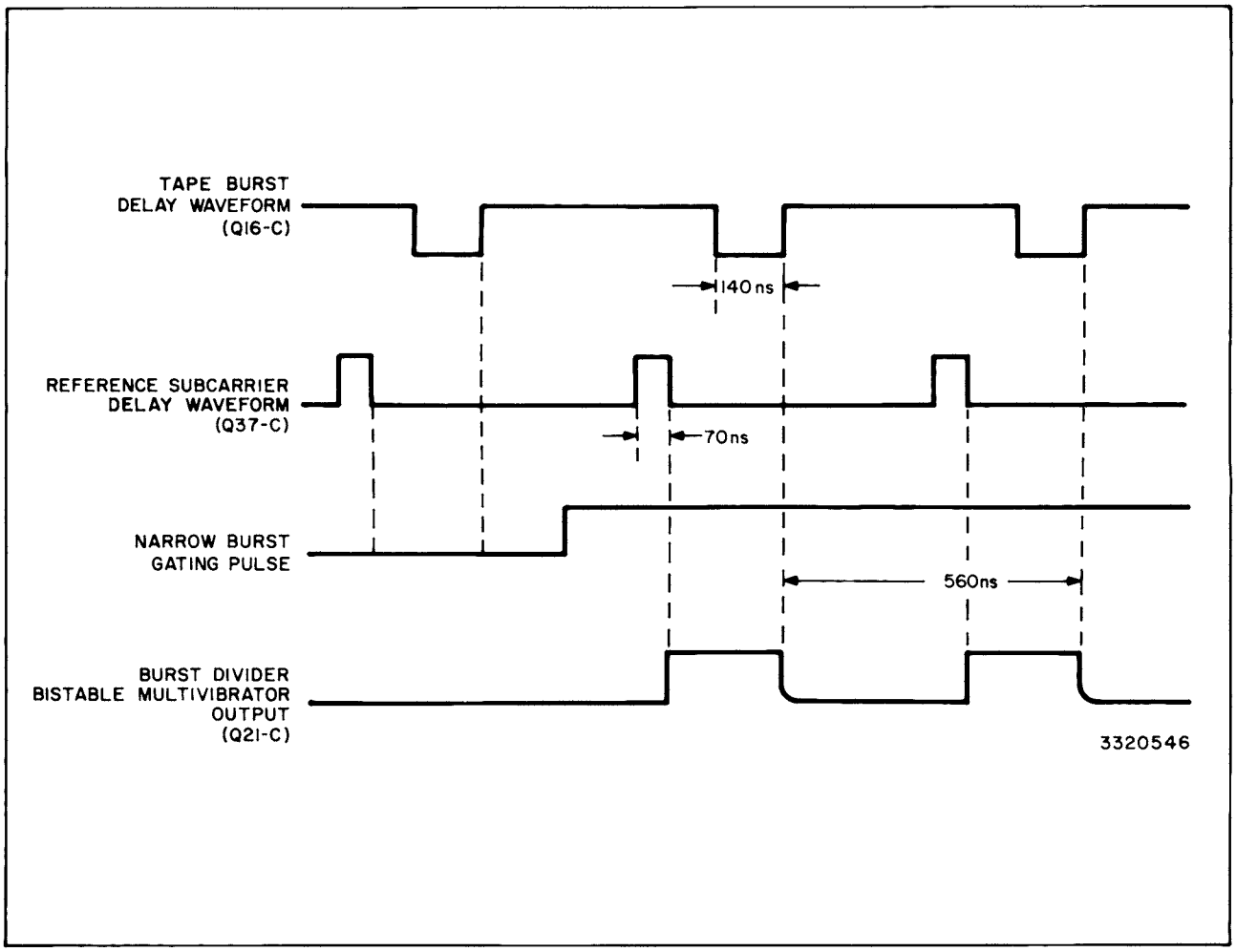
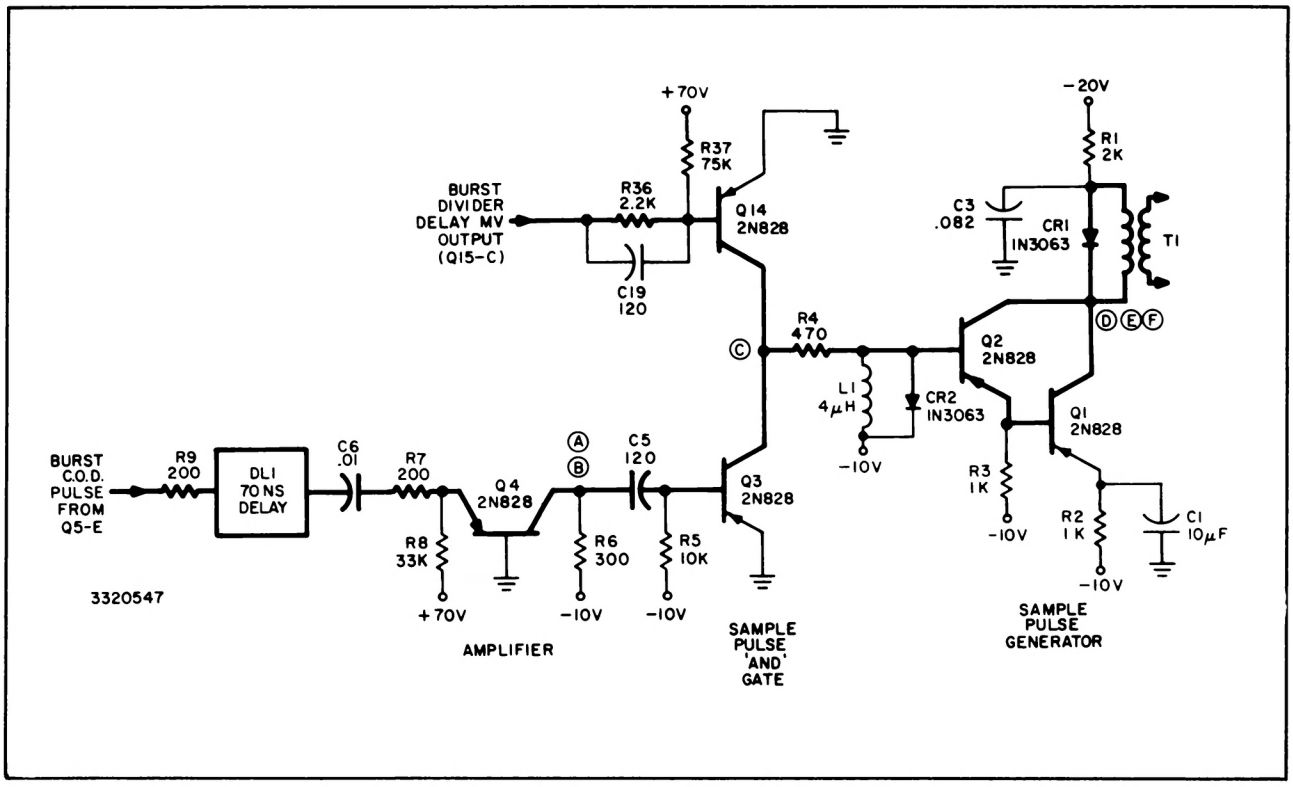


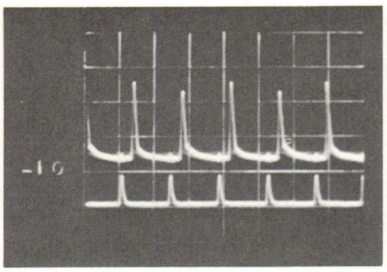
Figure 60—Burst Divider Bistable Multivibrator Timing Diagram

by current withdrawn from its base by the −6.8 volt potential via resistors R61, R62 and inductor L7, and the collector potential of Q21 goes to ground. When the collector of transistor Q21 is at ground potential diode CR11 is forward biased by the positive potential applied to its anode from the divider network consisting of resistors R60 and R57 connected between the +70 volt supply and ground, and transistor Q22 is held in cut-off by the contact potential of the diode. The multivibrator will remain in this state until a reset pulse drives the collector potential of transistor Q22 to ground.

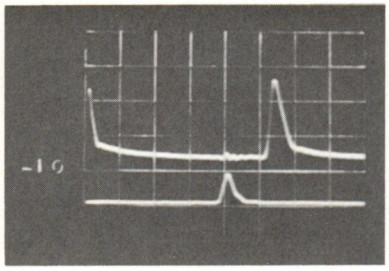
When a reset pulse occurs and drives the collector of transistor Q22 to ground potential, diode CR9 is forward biased once again by the positive potential applied to its anode and transistor Q21 is biased into cut-off by the contact potential of the diode. When transistor Q21 is cut off, ground potential is removed from its collector and transistor Q22 is biased into saturation by current withdrawn from its base by the −6.8 volt potential via resistors R56 and R57. The multivibrator will then remain in this state until the next positive-going set pulse appears at the base of transistor Q22.

The resulting output at the collector of transistor Q21 is a rectangular waveform having a negative-going edge timed to the trailing edge of the 140 nanosecond tape burst delay waveform and a positive-going edge timed to the trailing edge of the 70 nanosecond reference subcarrier delay waveform, as shown on the *Burst Divider Bistable Multivibrator Timing Diagram* (figure 60). Capacitors C26 and C28 and inductor L7 provide more positive transistor switching, and thereby insure that the output rectangular waveform will have sharply defined timing edges. The bistable multivibrator output waveform, shown in figure 57F, is fed to the base of transistor Q20 in the burst divider 'AND' gate circuit.

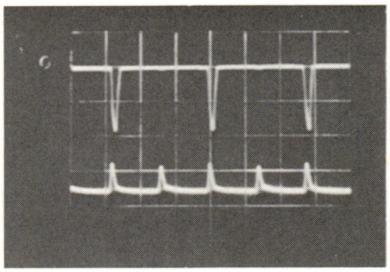




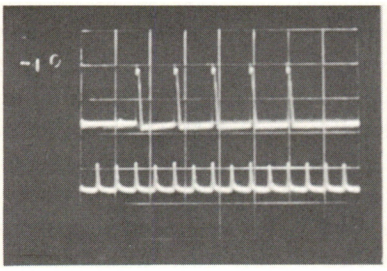
A. Top: Q4 collector, 2v/cm.
Bottom: Q5 emitter, 10v/cm.



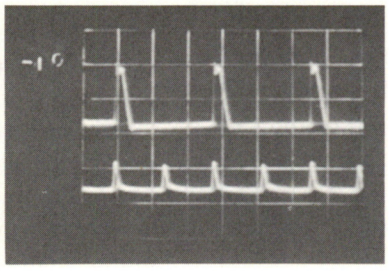
B. Top: Q4 collector, 2v/cm.
Bottom: Q5 emitter, 10v/cm.
(.05 μsec/cm)



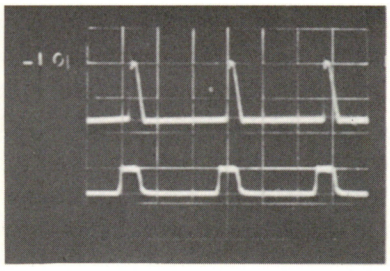
C. Top: Q3 collector, 5v/cm.
Bottom: Q4 collector, 5v/cm.



D. Top: Q2 collector, 5v/cm.
Bottom: Q4 collector, 5v/cm.
(0.5 μsec/cm)



E. Top: Q2 collector, 5v/cm.
Bottom: Q4 collector, 5v/cm.



F. Top: Q2 collector, 5v/cm.
Bottom: Q15 collector, 5v/cm.

Machine in STOP mode (back-to-back signal). All sweep times 0.2 μsec/cm unless otherwise noted.

Figure 61—Sample Pulse Generator

Sample Pulse Generator

To obtain optimum color ATC system performance it is desirable to utilize the sharp leading edge of the burst C.O.D. pulse in generating the sample pulse and to obtain approximately five sample pulses during each TV line. In the sample pulse generator circuit shown in figure 61, the burst C.O.D. pulse and the 140 nanosecond pulse from transistor Q15 in the burst divider delay multivibrator are fed to an 'AND' gate which produces the sample pulse. As explained above in the *Tape Burst Divider and Delay Circuit* discussion, the 140 nanosecond pulse occurs at one-half the tape burst frequency during the narrow burst interval and has a leading edge which is timed to the leading edge of the burst C.O.D. pulse. In order to prevent the loss of the sharp leading edge of the burst C.O.D. pulse which would occur if the 'AND' gate were triggered by the leading edges of the burst C.O.D. pulse and 140 nanosecond pulse simultaneously, the burst C.O.D. pulse is passed through a 70 nanosecond fixed delay before being fed to the 'AND' gate and thus appears at the 'AND' gate approximately half way through the 140 nanosecond pulse interval. Since the 140 nanosecond pulse occurs only during the narrow burst gating pulse interval, the number of sample pulses actually produced depends upon the width of the narrow burst pulse. The width of the narrow burst pulse is in turn determined by the setting of the BURST GATE WIDTH potentiometer in the chroma separator module, and an average BURST GATE WIDTH potentiometer setting results in the generation of approximately five sample pulses. Therefore the desired conditions are met; i.e., approximately five sample pulses per TV line are produced and each pulse is triggered in effect by the leading edge of the burst C.O.D. pulse.

The input signal to delay line DL1 is the tape burst C.O.D. pulse from emitter follower transistor Q5. This pulse is positive-going and occurs at the burst frequency, as shown on the *Sample Pulse Timing Diagram* (figure 62). Delay line DL1 provides a fixed delay of approximately 70 nanoseconds, and the delayed burst C.O.D. pulse is coupled to common base amplifier transistor Q4. Transistor Q4 provides a convenient means of terminating the delay line with a slight amount of non-inverting gain to recover any delay line losses. The output pulse at the collector of transistor Q4 occurs at the tape burst frequency (figure 61A) and has a sharp positive-going leading edge which is delayed 70 nanoseconds with respect to the leading edge of the burst C.O.D. pulse due to the action of delay line DL1. (See figure 61B and the timing diagram, figure 62.) Transistor Q3, normally biased into saturation by current withdrawn from its base by the −10 volt supply via resistor R5, is driven into cut-off by the sharp positive-going spike resulting from the differentiation of the rapid positive-going edge of the amplified pulse. When transistor Q3 is driven into cut-off its collector potential is determined by the state of transistor Q14 since the collectors of both transistors are common.

Transistors Q3 and Q14 form the sample pulse 'AND' gate which produces an output pulse only when both transistors are simultaneously in the cut-off state. Transistor Q3 is controlled by the delayed burst C.O.D. pulse, as explained above, and transistor Q14 is controlled by the output from transistor Q15 in the burst divider delay multivibrator circuit. The output signal from transistor Q15 is a 140 nanosecond pulse which occurs at one-half the tape burst frequency during the narrow burst interval. During the interval between 140 nanosecond pulses the collector potential of transistor Q15 is approximately −4 volts and transistor Q14 is biased into saturation by current withdrawn from its base by the −4 volt potential. During the 140 nanosecond pulse interval, the collector potential of transistor Q15 is ground and transistor Q14 is then biased into cut-off by the positive potential applied to its base from the divider network consisting of resistors R36 and R37 connected between +70 volts and ground. When transistors Q14 and Q3 are simultaneously in the cut-off state their common collector potential falls to approximately −9 volts and a negative-going output pulse is thereby produced (figure 61C).

Since transistor Q14 is cut off by a positive-going edge which has been derived from the positive-going leading edge of the burst C.O.D. pulse and transistor Q3 is cut off by a pulse which is also derived from the leading edge of the burst C.O.D. pulse but is delayed by approximately 70 nanoseconds, both transistors will be in the cut-off state at a point approximately half way through the 140 nanosecond pulse interval. (Refer to the timing diagram, figure 62.) Therefore the negative-going pulse output from the sample pulse 'AND' gate is derived from the positive-going leading edge of the burst C.O.D. pulse and occurs at one-half the tape burst frequency.

Inductor L1 in the collector circuit of transistors Q14-Q3 would normally produce a "ringing" effect when energized by the negative-going 'AND' gate output pulse. However, after the first half cycle

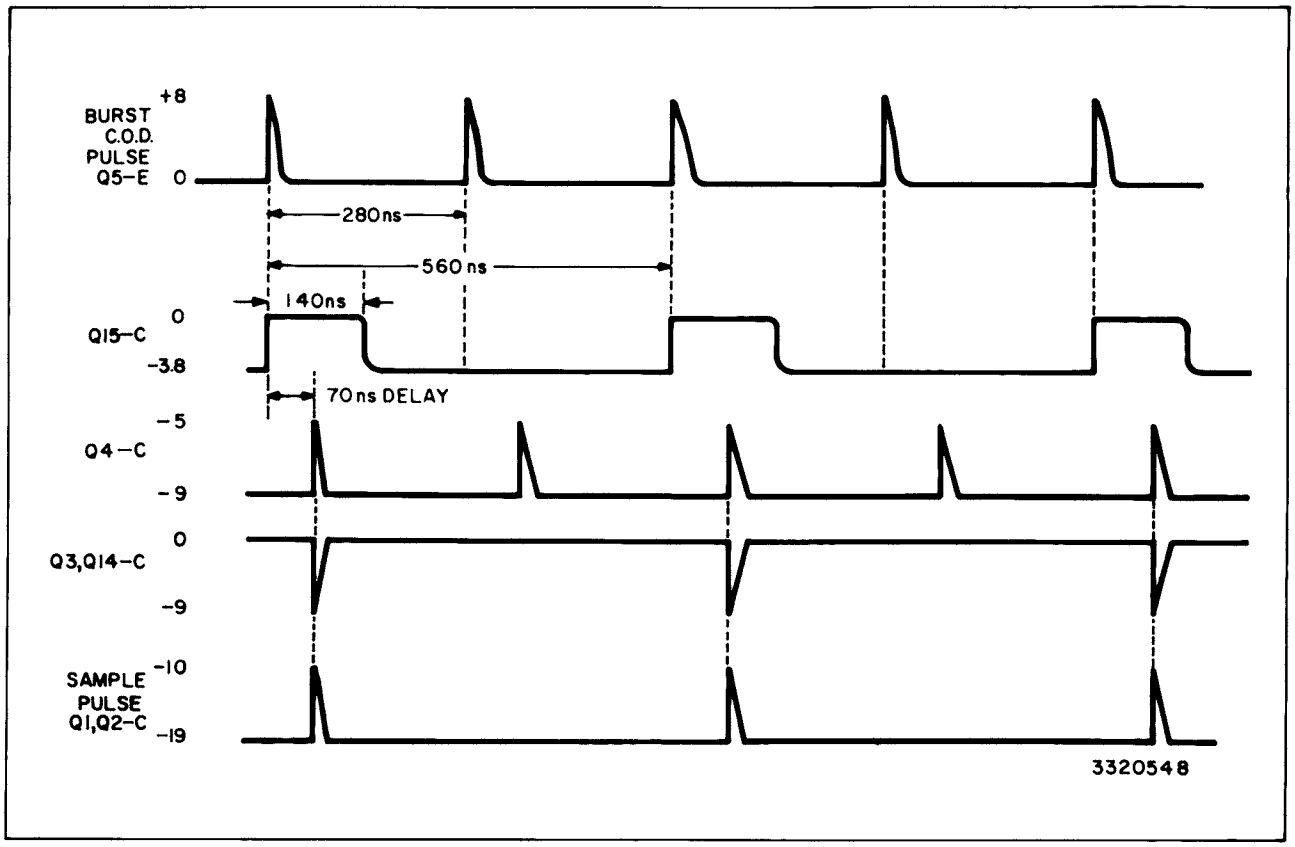


Figure 62—Sample Pulse Timing Diagram

(negative-going pulse) has occurred, the positive-going half cycle which would normally follow forward biases diode CR2 and thereby bypasses the inductor and ends the ringing action. Inductor L1 thus provides a high frequency peaking action which insures that the sample pulse 'AND' gate output will have a rapid negative-going (leading) edge. This edge is utilized in triggering transistor Q2 in the sample pulse generator circuit.

During the interval between negative-going 'AND' gate pulses the common collector potential of 'AND' gate transistors Q14-Q3 is ground. Therefore, during this interval the potential applied to the base of transistor Q2 from the divider network consisting of inductor L1 and resistor R4 connected between −10 volts and ground is positive with respect to the emitter potential of Q2 and the transistor is cut off. When transistor Q2 is cut off its emitter potential is −10 volts and, since this potential is applied directly to the base of transistor Q1, transistor Q1 is also biased into cut-off. During the interval between 'AND' gate pulses then, transistors Q2 and Q1 are both cut off and their common collector potential is approximately −20 volts. The negative-going leading edge of the 'AND' gate pulse drives transistor Q2 into conduction, and the resulting negative-going pulse appearing at the emitter of Q2 drives transistor Q1 into conduction. Thus transistors Q2 and Q1 are in effect driven into conduction simultaneously by the leading edge of the delayed burst C.O.D. pulse. When transistors Q2 and Q1 are driven into conduction their common collector potential rises to approximately −10 volts and a positive-going pulse, designated the phase sample pulse, is thereby produced (figures 61D, E, and F).

Transistors Q2 and Q1 provide the current required to drive pulse transformer T1 and at the same time maintain a high degree of isolation between bypass capacitor C1 and the input circuit to transistor Q2. Diode CR1 is connected across the primary winding of transformer T1 in such a manner that any negative-going signal excursions which may appear at the common collector of transistors Q2-Q1 will forward bias the diode, thereby effectively short-circuiting the primary winding and thus suppressing inductive kickback, etc. The positive-going sample pulse appearing at the primary of transformer T1 is coupled by the transformer to the error detector circuit.

Phase Error Detector

The phase error detector circuit shown in figure 63 produces a varying error signal which bears a direct relationship to the difference in phase between the tape burst and reference subcarrier signals when the machine is playing back tape normally in the color ATC mode. The error signal produced by the detector circuit is utilized in the color processor module in establishing the PEB (positive error bus) and NEB (negative error bus) potentials which in turn control the delay developed by the electronically variable video delay line in the color delay module. In TR-22 machines, the error signal output is also fed to the CRO monitor switcher for presentation on the CRO monitor.

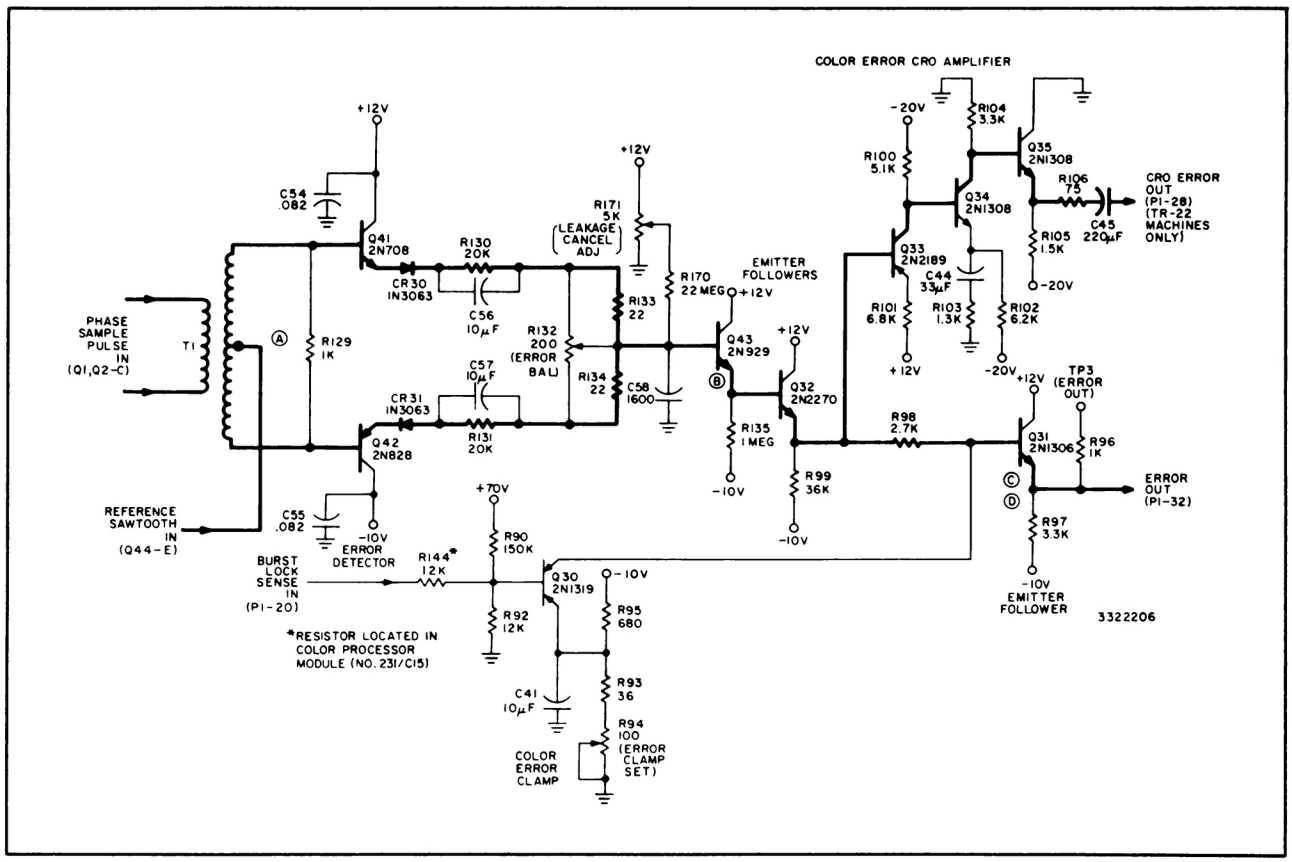
The method of error detection employed by the circuit consists of sampling the linear portion of a sawtooth waveform slope and charging a storage capacitor to the potential on the slope at the instant of sampling. The sample pulse is derived from the tape burst signal and the sawtooth waveform is derived from the reference subcarrier signal; however, to insure that sampling will occur only over the linear portion of the sawtooth waveform slope, both the sample pulse and sawtooth waveform occur at one-half the burst (subcarrier) rate and logic circuits are utilized in determining the sample pulse timing as explained in the preceding circuit discussions. The center of the sawtooth waveform slope corresponds to the zero error reference point; therefore, as the phase difference between the tape burst and reference subcarrier signals increases the sample pulse will move higher or lower on the slope (depending upon the relative phase of the burst and subcarrier signals) and the error signal will increase in a positive or negative direction respectively.

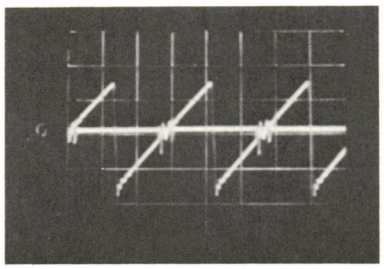
Approximately five samplings will be obtained during each TV line and the instantaneous potentials obtained at each sampling are averaged in later circuitry to form the final error signal. Since the error detector circuit functions properly only when a tape burst signal is present, a special clamping circuit produces a steady signal corresponding to zero error if for any reason there is no tape burst signal. Thus the clamping circuit protects the error control circuitry from being affected by noise or other spurious signals during any condition other than tape playback in the color ATC mode.

The positive-going sample pulse appearing at the primary winding of pulse transformer T1 is superimposed upon the slope of the reference sawtooth waveform which is fed to the center-tap of the transformer secondary winding. Transformer T1 splits the phase of the sample pulse, and pulses of opposite polarity are simultaneously fed from each end of the transformer secondary winding directly to the bases of transistors Q41 and Q42 which are normally in the cut-off state. The pulse fed to the base of transistor Q41 is positive-going and the pulse fed to the base of transistor Q42 is negative-going; therefore, when a sample pulse appears the transistors are driven into conduction to a greater or lesser degree as determined by the sample pulse position on the reference sawtooth waveform slope.

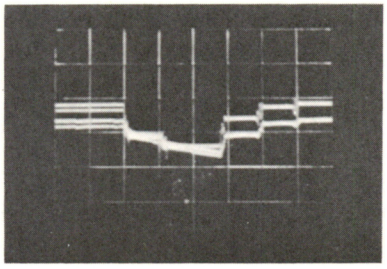
Assuming zero phase error, the sample pulse will sample at the center of the sawtooth waveform slope and pulses of equal amplitude and opposite polarity will drive transistors Q41 and Q42 into conduction. Current will then flow from the +12 volt supply to the −10 volt supply via transistors Q41 and Q42 and the resistors and diodes connected between the transistors. Potentiometer R132 is utilized in varying the current flow through the series circuit to obtain zero potential at the junction of resistors R133 and R134 (figure 63A). Zero (ground) potential at the junction of resistors R133 and R134 results in zero charge across storage capacitor C58 and ground potential at the base of transistor Q43. Capacitors C56 and C57 act to smooth out the voltage fluctuations through resistors R130 and R131 respectively as current pulses flow in the series circuit. Thus essentially steady d-c emitter biasing potentials, representing the average voltage drop across each resistor, are developed across each capacitor. These potentials set the operating points of transistors Q41 and Q42 at levels which allow only the tip of the pulse fed to the base of each transistor to drive the transistor into conduction. This protects against an erroneous error signal by insuring that the transistors cannot be driven into conduction by either the positive- or negative-going extremity of the sawtooth waveform itself.

As the phase error increases in such a manner that the sample pulse moves up on the sawtooth waveform slope (i.e., in a positive direction), the relative amplitudes of the pulses fed to the bases of transistors Q41 and Q42 will change so that Q41 will conduct more heavily and the conduction of Q42 will be decreased correspondingly when a sample pulse appears. (When the sample pulse approaches its extreme positive position on the sawtooth waveform slope, the emitter biasing potential developed across capacitor C57 will be sufficient to hold transistor Q42 in the cut-off state during the entire sampling interval.) As the conduction of transistor Q41 is increased, a greater portion of the emitter current of Q41 flows into storage capacitor

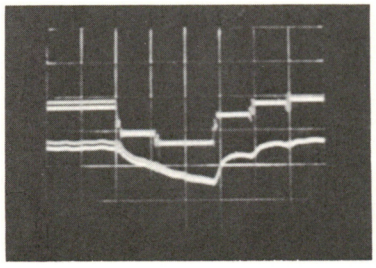




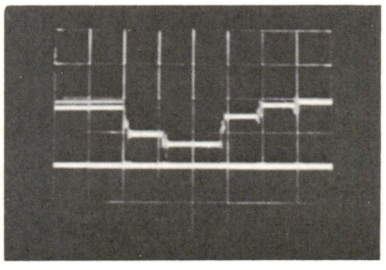
A. Top: T1-5, 1v/cm.
Bottom: Jct. R132-R134, 1v/cm.
(0.2 μsec/cm)



B. Top: Q43 emitter, 1v/cm.
Bottom: Jct. R132-R134, 1v/cm.
Cracking.



C. Top: Jct. R132-R134, 1v/cm.
Bottom: Q31 emitter, 1v/cm.
Cracking.



D. Top: Jct. R132-R134, 1v/cm.
Bottom: Q31 emitter, 1v/cm.
Cracking clamped.

Machine in STOP mode (back-to-back signal). All sweep times 0.5 μsec/cm unless otherwise noted.

Figure 63—Phase Error Detector and Output Circuit

C58. Thus after one or two sample pulses have occurred, capacitor C58 charges to the positive potential on the sawtooth waveform slope at the instant of sampling.

Conversely, as the phase error increases in such a manner that the sample pulse moves down on the sawtooth waveform slope (i.e., in a negative direction), transistor Q42 will conduct more heavily and the conduction of transistor Q41 will be decreased correspondingly when a sample pulse appears. (When the sample pulse approaches its extreme negative position on the sawtooth waveform slope, the emitter biasing potential developed across capacitor C56 will be sufficient to hold transistor Q41 in the cut-off state during the entire sampling interval.) As the conduction of transistor Q42 is increased a greater portion of the emitter current of Q42 flows from storage capacitor C58. Thus after one or two sample pulses have occurred, capacitor C58 charges to the negative potential on the sawtooth waveform slope at the instant of sampling.

The d-c potential developed across capacitor C58 is applied directly to the base of emitter follower transistor Q43. This potential, corresponding to the potential on the sawtooth waveform slope at the instant of sampling, may vary between the approximate limits of +1 volt and −1 volt as the sample pulse moves over its allowable range. Therefore, since the emitter of NPN transistor Q43 is returned to the −10 volt supply via resistor R135 the potential at its base will always be positive with respect to −10 volts and the transistor will conduct continuously. The base current of transistor Q43 is provided by the +12 volt potential via potentiometer R171 and resistor R170, thereby preventing Q43 from "loading" storage capacitor C58. Due to the very high impedances of resistors R170 and R135, capacitor C58 is in effect isolated from transistor Q43 and will therefore retain its charge from one TV line to the next without decay.

Since emitter follower transistor Q43 is continuously biased into conduction, the instantaneous d-c potentials applied to its base during the sampling intervals will appear at its emitter. Figure 63B shows the error signal at the emitter of transistor Q43 when a "cracking effect" has been artificially created while operating the machine in the STOP mode with a back-to-back color signal. (The "cracking effect" is explained briefly in the general discussion at the beginning of the color error detector module circuit description, and in more detail in the *System Functional Description* section.) Transistor Q32 also functions as an emitter follower and is biased into conduction by current withdrawn from its base by the −10 volt potential in its emitter circuit. Transistors Q43 and Q32 in series provide sufficient isolation to prevent the output circuits from loading the error detector circuit and also provide the current required to drive the color error output circuit and, in TR-22 machines, the parallel color error CRO amplifier circuit.

During normal tape playback in the color ATC mode, the error signal appearing at the base of color error output transistor Q31 is the fluctuating output signal from the error detector circuit. However, in the absence of a tape burst signal it is desirable to provide output transistor Q31 with a steady signal which corresponds to zero error. The steady zero error signal is provided by the color error clamp circuit which in turn is controlled by the burst lock sense signal fed to the module at pin 20 of plug P1 from the color processor module (no. 231/C15).

When the machine is playing back tape normally in the color ATC mode, the burst lock sense signal is ground potential. The potential applied to the base of transistor Q30 is then approximately +2.7 volts due to the action of the voltage divider network consisting of resistor R90 and resistors R92 and R144 in parallel connected between +70 volts and ground. (Note in figure 63 that resistor R144 is located in the color processor module.) Transistor Q30 is a PNP bilateral type (i.e., either electrode may function as emitter or collector, depending upon the biasing arrangement), however the +2.7 volt potential applied to its base remains positive with respect to the potential appearing on either electrode and the transistor is cut off. Thus when the machine is playing back tape normally in the color ATC mode transistor Q30 is cut off and has no effect on the error signal output.

If a tape burst signal is not present for any reason, or the machine has failed to "lock-up" in the pixlock servo mode, the burst lock sense signal is a negative potential. Transistor Q30 is then biased into saturation by current withdrawn from its base by the negative potential. In figure 63, the potential applied to the lower electrode of transistor Q30 from the divider network consisting of resistors R95 and R93 and potentiometer R94 connected between −10 volts and ground is determined by the setting of R94 and may fall within the approximate limits of −0.5 and −1.5 volts dc. If the momentary error signal appearing at the junction of resistors R133 and R134 is negative with respect to the potential applied to the lower electrode of transistor Q30 from the divider network, the lower electrode

acts as the emitter and the upper electrode as the collector. Since transistor Q30 is a bilateral type, if the momentary error signal at the junction of resistors R133 and R134 is positive with respect to the potential applied to the lower electrode of Q30 the upper electrode acts as emitter and the lower electrode as collector. In either case the base of emitter follower transistor Q31 is clamped at the potential appearing at the junction of resistors R95 and R93 when clamping transistor Q30 is saturated.

As mentioned above, the potential appearing at the junction of resistors R95 and R93 depends upon the setting of potentiometer R94 (ERROR CLAMP SET). The proper setting of potentiometer R94 is that setting which establishes PEB and NEB potentials of −7.1 and −12.9 volts respectively in the color processor module. These potentials represent a potential difference of 2.9 volts between the video delay line mid-point and both the PEB and NEB, and thus correspond to a zero error signal. Therefore, when potentiometer R94 is correctly set the clamping circuit insures that a fixed d-c potential, equivalent to a zero error signal, will be applied to the video delay line in the color delay module when the tape burst signal is not present. (The proper method of adjusting potentiometer R94 is presented in the *Adjustment* section at the end of the module circuit description.)

Transistor Q31, biased into conduction continuously by current withdrawn from its base by the −10 volt potential in its emitter circuit, isolates the error detector circuit from the output load and provides the current required to drive the load. The output error signal is fed via pin 32 of plug P1 to the color processor module and may be observed at test point TP3 (ERROR OUT). Figure 63C shows the error signal at the emitter of transistor Q31 when the cracking effect has been artificially created, while figure 63D shows the effect of the color error clamp circuit on the output error signal.

The error signal appearing at the emitter of transistor Q32 is also fed to the color error CRO amplifier circuit. Transistors Q33 and Q34 amplify the error signal and transistor Q35, functioning as an emitter follower, provides the low output impedance which is required to drive the CRO monitor. In TR-22 machines the output signal at the emitter of transistor Q35 is fed via pin 28 of plug P1 directly to the CRO monitor switcher, and the error signal may be observed on the CRO monitor when the CATC ERROR pushbutton on the monitor switcher is depressed. The gain of transistors Q33 and Q34 is fixed to provide approximately 100 IRE units of deflection for an error of 280 nanoseconds (360°).

Adjustments

The following color error detector module adjustment procedures are part of the color ATC system setup adjustments and, with the possible exception of the color error gain potentiometer, once set they should not normally require readjustment. Test equipment required when making the adjustments consists of a vacuum-tube voltmeter such as the *RCA Type WV-98A Voltohmyst* or the equivalent, and a dual-trace oscilloscope. The *Tektronix Type 585-A* oscilloscope, or the equivalent, is recommended for obtaining the most accurate adjustments; however, satisfactory results may be obtained by utilizing the *Tektronix Type 535-A* or *Type 545-A* oscilloscope or the equivalent.

Color Error Gain

1a. In TR-22 machines rotate the FM standards switch (module no. 205) to COLOR STD 1 or 2 position; in TR-3 machines rotate the demodulator output switch (module no. A18) to COLOR position; in TR-4 machines rotate both the demodulator output switch and the modulator switch (module nos. A18 and A2) to COLOR position.

b. In all machines rotate the mode selector switch on the ATC delay/output module (no. 223/B11) to COLOR ATC or NON-PHASED COLOR position.

2. Feed a 3.58 mc subcarrier (4.43 mc subcarrier if the machine is operated on 625-line standards) and sync to the machine, and play back a tape containing a color bar signal (split field with 100% white bar) in the pixlock servo mode.

3. In TR-22 machines, connect a color monitor and/or vectorscope to jack J17 (COLOR MONITOR OUT) at the front of the machine.

In TR-3 or TR-4 machines, connect a color monitor and/or vectorscope to one of the VIDEO OUT jacks at the rear of the machine.

4. Connect external oscilloscope probe to ERR OUT test point on module front panel or, in TR-22 machines, press CATC ERR pushbutton on the CRO monitor switcher.

5. Manually decrease the vacuum guide pressure.

6. While observing the external oscilloscope or CRO monitor reduce the monochrome ATC error gain slightly, utilizing the ERR GAIN screwdriver control on the ATC reference module (no. 226/B14) front panel, so that some guide error appears in the color signal. (*Do not exceed the range of the color error signal; i.e., 100 IRE units.*)

7. Depress the COLOR OUT pushbutton on the picture monitor switcher.

8. Adjust the COLOR ERR GAIN screwdriver control on the module front panel for best correction of the color picture as observed on the vectorscope or color monitor. (The COLOR ERR GAIN control is properly set when, while observing the vector display on the vectorscope, minimum jitter of the burst vector is obtained.)

NOTE: The residual error from monochrome ATC must not exceed the range of the color error signal (100 IRE units), as observed in step 6 above.

9. Re-adjust the ERR GAIN screwdriver control on the ATC reference module front panel for proper correction, and then re-adjust the vacuum guide to its normal position.

Machine Setup

In the adjustment procedures outlined below, the most precise adjustments will be obtained when the machine is operated in the STOP mode with a back-to-back signal. To set up the machine for operation in the STOP mode with a back-to-back signal, proceed in the following manner:

1. In TR-22 machines rotate the FM standards switch (module no. 205) to COLOR STD 1 or 2 position; in TR-3 machines rotate the demodulator output switch (module no. A18) to COLOR position; in TR-4 machines rotate both the demodulator output switch and the modulator switch (module nos. A18 and A2) to COLOR position.

2. In all machines rotate the mode selector switch on the ATC delay/output module (no. 223/B11) to COLOR ATC or NON-PHASED COLOR position.

3. In TR-22 and TR-4 machines feed a color bar signal (split field with 100% white bar), 3.58 mc subcarrier (4.43 mc subcarrier if machine is operated on 625-line standards), and sync to the machine, and operate the machine in STOP mode (MOD-DEMOD). In TR-3 machines, remove the ATC video out pins (nos. 14 and 30) from the demodulator output module receptacle at the rear of the machine; feed a 1 volt peak-to-peak color signal, subcarrier, and sync to the machine; and operate the machine in STOP mode.

Tuned Circuit Inductor L4

1. Place the color error detector module on the module extender so that the side on which inductor L4 is mounted faces upward. (Place a flat metal plate, wrapped with tape to protect the components, over the module to simulate inter-module shielding.)

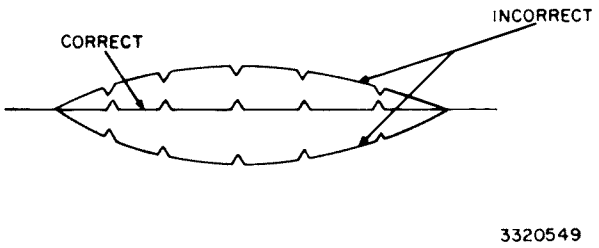


Figure 64—Correct and Incorrect Tuning of Inductor L4

2. Set up the machine as instructed in the *Machine Setup* procedure or, if the machine is to be operated in the PLAY mode, refer to the alternate procedure beginning with step 5 below.

3. Connect external oscilloscope probe to junction of resistors R133 and R134.

4. While observing the sampling interval on the oscilloscope, tune inductor L4 so that the intervals between sampling pips are flat. (See figure 64.)

5. If it is desired to operate the machine in the PLAY mode, set up the machine as instructed in steps 1 and 2 of the *Color Error Gain* adjustment procedure above and proceed with steps 6 and 7 below.

6. Connect a vectorscope to one of the VIDEO OUT jacks at the front of the machine (at the rear of the TR-3 or TR-4 machines) or, connect an external oscilloscope probe to the junction of resistors R133 and R134.

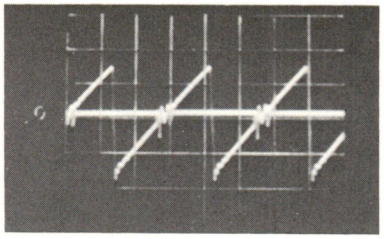
7. If a vectorscope is used, tune inductor L4 for minimum spread on one of the color bar vectors. If the external oscilloscope is used, tune inductor L4 so that the intervals between sampling pips are flat. (See figure 64.)

Error Balance

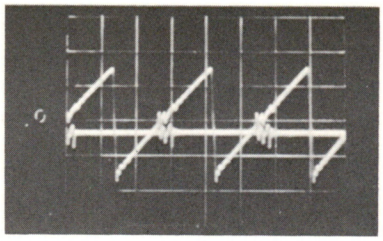
1. Place the error detector module on the module extender so that the side on which potentiometer R132 is mounted faces upward.

2. Set up the machine as instructed above in the *Machine Setup* procedure, or if it is desired to operate the TR-3 machine in PLAY mode set up the machine as instructed in steps 1 and 2 of the *Color Error Gain* adjustment procedure above.

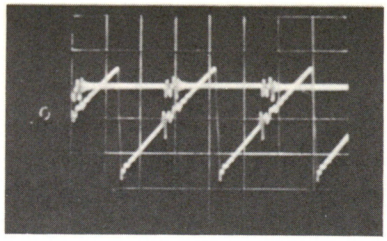
3. Connect both external oscilloscope probes to terminal 5 of transformer T1, and set the oscilloscope sweep for a subcarrier rate presentation. Set the oscilloscope for a DC input on each probe and match the probes for vertical gain and vertical position (approximately 0.5 volt/cm).



A. Top: T1-5, 1v/cm.
Bottom: Jct. R132-R133, 1v/cm.
ERROR BAL correctly adjusted.



B. Top: T1-5, 1v/cm.
Bottom: Jct. R132-R133, 1v/cm.
ERROR BAL max clockwise.



C. Top: T1-5, 1v/cm.
Bottom: Jct. R132-R133, 1v/cm.
ERROR BAL max counterclockwise.

Machine in STOP mode (back-to-back signal). All sweep times 0.2 μsec/cm.

Figure 65—Error Balance Adjustment Waveforms

4. Expand the oscilloscope sweep rate to 0.1 μsec/cm and adjust the SYSTEM PHASE control on the color phase module (no. 232/C16) front panel so that the pip (appearing during the burst interval) falls at the center of the slope. (If the error clamp adjustment is being made on a TR-3 machine operating in the PLAY mode the SYSTEM PHASE control will have no effect on centering the pip. In this case expand the oscilloscope sweep rate to 0.1 μsec/cm and proceed to step 5.)

5. Remove one of the external oscilloscope probes from terminal 5 of transformer T1 and connect it to the junction of resistors R133 and R134.

6. Adjust potentiometer R132 so that the d-c signal at the junction of resistors R133 and R134 falls at the same level as the pip on the slope. (In TR-3 machines operating in the PLAY mode, the d-c signal will be observed as a band of horizontal lines and a precise setting of potentiometer R132 will be difficult to attain. However, satisfactory results may be attained by adjusting R132 so that the band of horizontal lines is superimposed upon the sampling range of the pip on the slope.) Figure 65A shows the waveform obtained when potentiometer R132 is correctly adjusted, while figure 65B shows the waveform obtained with R132 rotated maximum clockwise and figure 65C shows the waveform obtained with R132 rotated maximum counterclockwise.

Error Clamp Set

IMPORTANT: The following error clamp set potentiometer adjustment can be accurately made only if the color processor module adjustments have been completed according to the color NLA adjustment procedure.

1. Place the color error detector module on a module extender so that the side upon which potentiometer R94 is mounted faces upward.

NOTE: Potentiometer R94 is mounted directly beneath potentiometer R171.

2. Place the color processor module (no. 231/C15) on a module extender.

NOTE: Since the color processor and color error detector modules are adjacent in TR-3/TR-4 machines, it will not be possible to place both modules on extenders simultaneously. Therefore, in these machines it is necessary to make trial adjustments in step 5 below until the correct setting of potentiometer R94 is attained.

3. Set up the machine as instructed above in the *Machine Setup* procedure.

4. Connect the negative lead of the vacuum-tube voltmeter to pin 13 of plug P1 on the color processor module, and insert the VTVM probe into the PEB test point on the color delay module (no. 324/C12) front panel.

CAUTION: Make certain the VTVM case is insulated from ground when making this adjustment.

5. Adjust potentiometer R94 in the color error detector module to obtain a PEB potential of +2.9 volts dc with respect to the delay line reference (DLR) potential, as measured on the VTVM.

Leakage Cancellation

1. Place the color error detector module on a module extender so that the side on which potentiometer R171 is mounted faces upward.

NOTE: Potentiometer R171 is mounted directly on top of potentiometer R94.

2. Set up the machine as instructed above in the *Machine Setup* procedure.

3. Connect an external oscilloscope probe to the emitter of transistor Q32 and adjust the oscilloscope sweep for a horizontal rate presentation.

4. While observing the error signal on the oscilloscope adjust potentiometer R171 to obtain a straight, horizontal line between horizontal samples.

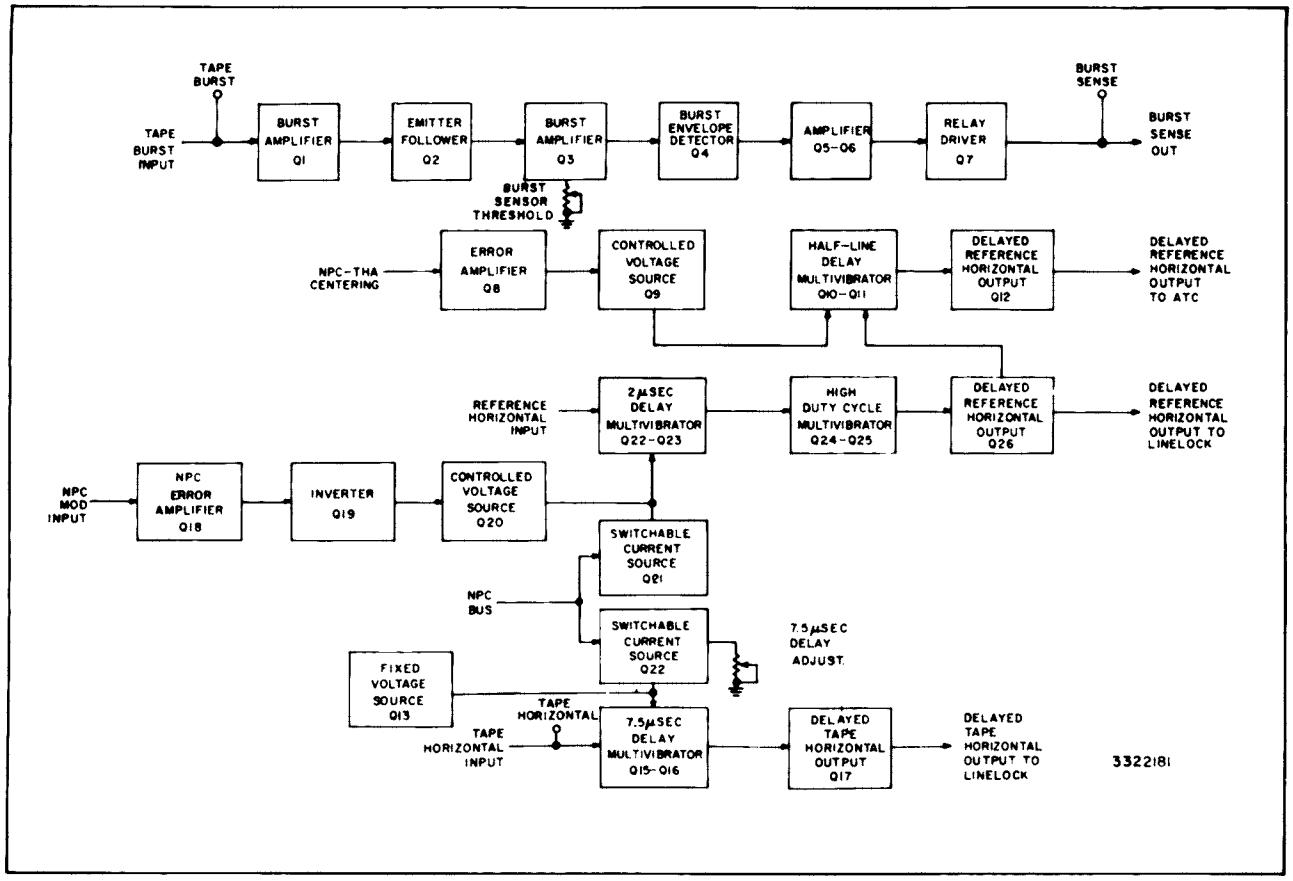


Figure 66—Color Sensor Module Block Diagram

COLOR SENSOR MODULE (323/C11)

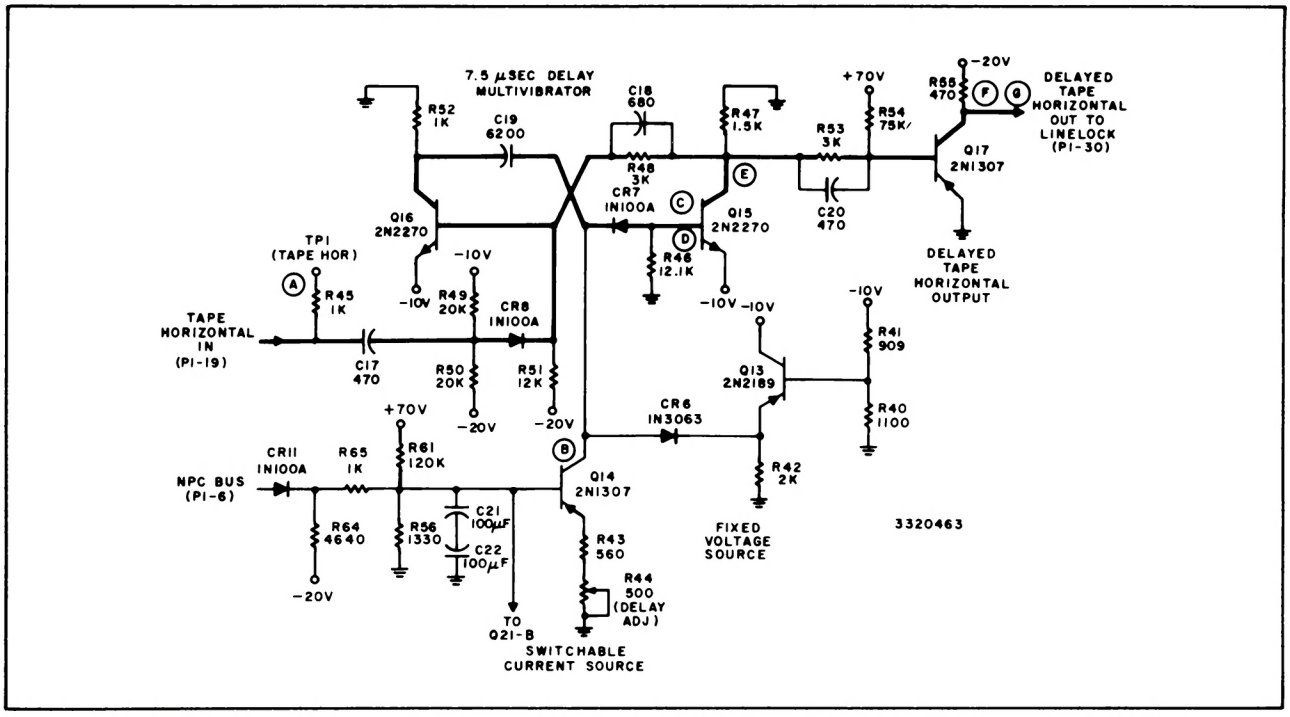
Circuit Description

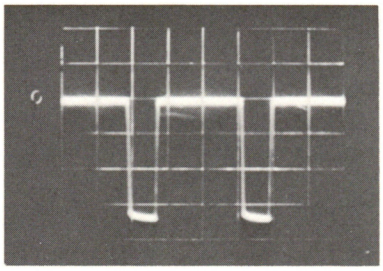
General

The color sensor module (no. 323/C11), shown in block diagram form in figure 66, performs two basic functions in the color ATC system. One function is to produce delayed tape and reference horizontal pulses which are utilized in developing the linelock error signal when the machine is playing back a tape in either the normal color ATC or non-phased color mode, and to produce a delayed reference horizontal pulse which is utilized in developing the ATC error signal when playing back a color tape in the non-phased color mode only. The other function performed by the color sensor module is to sense the presence of tape burst and, when burst is present, to produce a control voltage which allows the color ATC system to function normally. When burst is absent from the incoming tape signal, the control voltage is such that regenerated burst is removed from the output signal and the video delay line in the color delay module (no. 324/C12) is clamped at the center of its delay range.

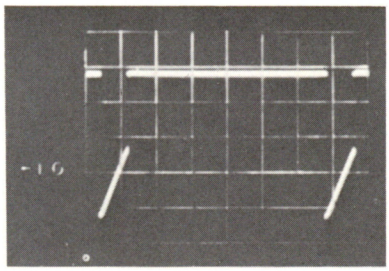
When the machine is playing back a color tape in the normal color ATC mode, the 7.5 microsecond delay multivibrator produces a pulse which is delayed with respect to tape horizontal by 7.5 microseconds and the 2 microsecond delay multivibrator produces a pulse which is delayed with respect to reference horizontal by 2 microseconds. Both the delayed tape and reference horizontal pulses are fed to the linelock module where the delayed tape horizontal pulse is utilized in the derivation of a sample pulse which samples the slope of a trapezoid waveform developed from the delayed reference horizontal pulse. The net difference of 5.5 microseconds between the delayed tape and reference horizontal pulses causes the head-wheel to advance in phase by that amount to compensate for delays introduced into the tape video path by the color ATC system.

During tape playback in the non-phased color mode the 7.5 microsecond delay multivibrator produces a pulse which is delayed by approximately 37 microseconds with respect to tape horizontal. The 2 microsecond delay multivibrator is controlled by the THAF (tape horizontal alignment, fine) error signal

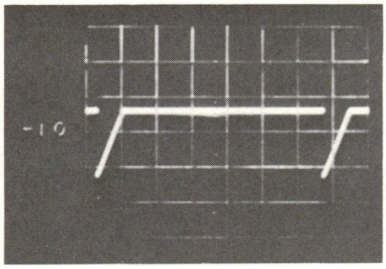




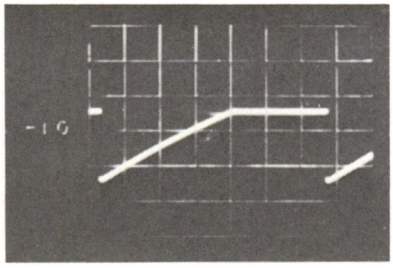
A. TP1 (TAPE HOR), 5v/cm. (20 μsec/cm)



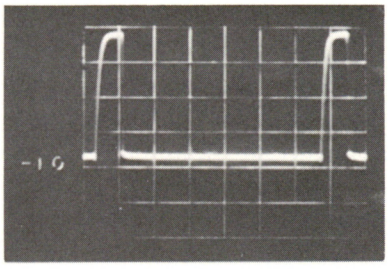
B. Q14 collector, 2v/cm.



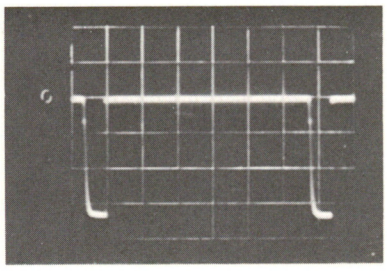
C. Q15 base, 2v/cm.



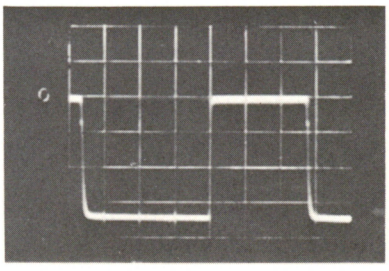
D. Q15 base, 2v/cm. NPC ground.



E. Q15 collector, 2v/cm.



F. Q17 collector, 5v/cm.



G. Q17 collector, 5v/cm. NPC ground.

Machine in STOP mode (back-to-back signal). All sweep times 10 μsec/cm unless otherwise noted.

Figure 67—Tape Horizontal Delay Circuit

developed in the color processor module and produces a pulse which is delayed with respect to reference horizontal by 30 ±20 microseconds as determined by the magnitude of the THAF error signal. These pulses are also fed to the linelock module where they perform the same functions as the delayed tape and reference horizontal pulses developed during tape playback in the normal color ATC mode.

In addition to the delayed tape and reference horizontal pulses fed to the linelock module, during non-phased color playback the delayed reference horizontal output pulse from the 2 microsecond delay multivibrator is fed to the half-line delay multivibrator. The half-line delay multivibrator is controlled by the THA (tape horizontal alignment) error signal developed in the monochrome ATC error detector module, and its purpose is to produce an output which is delayed with respect to the delayed reference horizontal pulse fed to the linelock module by one-half a TV line. Thus the reference horizontal output from the half-line delay multivibrator has been delayed by a total of one full TV line with respect to reference horizontal generated in the reference generator module (no. 312/B18). The half-line delay multivibrator output is fed to the monochrome ATC reference module where it is utilized in developing the ATC reference trapezoid waveform. Since the ATC sampling pulse is generated from tape horizontal, the full TV line delay insures that sampling will occur on the slope of the trapezoid waveform.

The color sensor module also includes a 46.4 K ohm resistor (R86) which is in series with the +70 volt supply and a normally open contact of NPC relay K32. When the machine is playing back a color tape in the non-phased color mode, NPC relay K32 is energized and a constant current is fed via the 46.4 K ohm resistor to current source transistor Q15 in the linelock module. Therefore, since the delay generator circuit of transistor Q1 in the linelock module is controlled by current source transistor Q15, during playback in the non-phased color mode the delay generated by transistor Q1 is fixed.

Tape Horizontal Delay

The purpose of the tape horizontal delay circuit, shown in figure 67, is to produce a positive-going edge which is delayed with respect to tape horizontal by 7.5 or 37 microseconds, depending upon whether the machine is playing back a color tape in the normal color ATC or the non-phased color mode respectively. The delay generated is equivalent to the timed cycle (unstable state) of a monostable multivibrator, and the multivibrator timed cycle is determined by the potential provided by a fixed voltage source in conjunction with current supplied by a switchable current source. The switchable current source is in turn controlled by the NPC bus potential, which is either −26 volts dc (when the ATC mode switch on the ATC delay/output module front panel is in COLOR ATC position) or ground (when the switch is in NON-PHASED COLOR position).

Tape horizontal fed to the module at pin 19 of plug P1 (figure 67A) is obtained from the tape sync processor module (no. 317/B20) and may be observed at test point TP1 (TAPE HOR). The incoming signal is differentiated by the network consisting of capacitor C17 and resistors R49 and R50, and the resulting positive- and negative-going spikes appear at the anode of diode CR8. Diode CR8 is normally reverse-biased by the −15 volt potential established at its anode by the divider network consisting of resistors R49 and R50, thus the negative-going spike resulting from the differentiation of tape horizontal has no effect on the diode. However the positive-going spike, corresponding to the positive-going (timed) edge of tape horizontal, forward biases diode CR8 and is thereby fed directly to the base of transistor Q16 in the delay multivibrator circuit.

Transistors Q15-Q16 and associated circuit components comprise the monostable delay multivibrator. In the multivibrator stable state transistor Q15 is saturated, transistor Q16 is cut off, and capacitor C19 is charged to a fixed potential of approximately −4.5 volts provided by voltage source transistor Q13. When the positive-going spike resulting from the differentiation of tape horizontal is applied to the base of transistor Q16 the transistor is driven into saturation and the multivibrator timed cycle (unstable state) begins. At the instant transistor Q16 is driven into saturation its collector potential falls to −10 volts and, since the voltage across capacitor C19 cannot change instantaneously, the potential at the cathode of diode CR7 falls to approximately −14.5 volts. This potential forward biases diode CR7, thereby cutting off transistor Q15, and capacitor C19 begins to charge utilizing current provided by transistor Q14 in addition to current flowing through resistor R46. When capacitor C19 has charged to a potential which is slightly positive with respect to −10 volts, transistor Q15 is biased into saturation once again and the timed cycle ends.

The timed cycle is determined by the fixed potential provided by voltage source transistor Q13 in conjunction with the magnitude of the charging current

supplied to capacitor C19. Transistor Q13 is biased into conduction continuously by a potential of −5.5 volts applied to its base from the divider network consisting of resistors R40 and R41, thus a fixed potential of approximately −5.3 volts will appear at its emitter. During the multivibrator stable state diode CR6 is forward-biased and capacitor C19 is charged to the fixed potential at the emitter of transistor Q13 minus the voltage drop across CR6, or approximately −4.5 volts. During the multivibrator timed cycle diode CR6 is reverse-biased and the fixed voltage source is cut off from the multivibrator timing circuit.

The magnitude of the charging current supplied to capacitor C19 during the multivibrator timed cycle is dependent upon the state of switchable current source transistor Q14, and Q14 is in turn controlled by the NPC bus potential applied to the module at pin 6 of plug P1. When the machine is playing back a color tape in the normal color ATC mode the NPC bus potential is −26 volts. This potential reverse-biases diode CR11 and a potential of approximately −3 volts applied to the base of transistor Q14 from the divider network consisting of resistors R56, R61, R64, and R65 biases Q14 into conduction. Transistor Q14 will then supply a constant current equal to the voltage on its emitter divided by the resistance of resistor R43 and potentiometer R44. As mentioned above, the charging current of capacitor C19 is the current flowing through resistor R46 plus the current supplied by transistor Q14. Therefore, during machine operation in the normal color ATC mode the charging current supplied to capacitor C19, in conjunction with the fact that the capacitor begins to charge from −14.5 volts, allows the capacitor to charge to the saturation potential of transistor Q15 in 7.5 microseconds (figures 67B and 67C). (The charging current supplied by transistor Q14 may be varied somewhat by adjusting DELAY ADJ potentiometer R44. However, once potentiometer R44 has been initially set for a multivibrator timed cycle of 7.5 microseconds, according to the procedure outlined under *Adjustments* at the end of the module circuit description, the potentiometer requires no further adjustment.) When the machine is playing back a color tape in the non-phased color mode the NPC bus is at ground potential. Diode CR11 is then forward-biased and a potential of approximately +1.5 volts applied to the base of transistor Q14 from the divider network biases Q14 into cut-off. In this case the charging path of capacitor C19 is through resistor R46 and diode CR7 only, and the multivibrator timed cycle is lengthened to 37 microseconds (figure 67D). Back-to-back capacitors C21 and C22, in the base circuit of transistor Q14, absorb the change in base potential when the machine is switched from one mode to the other, thus "softening" the switching action.

When capacitor C19 has charged to the saturation potential of transistor Q15, the collector potential of Q15 falls to −10 volts and a potential of −12 volts is applied to the base of transistor Q16 from the divider network consisting of resistors R48 and R51. This potential biases transistor Q16 into cut-off and the multivibrator timed cycle ends. At the instant transistor Q16 is cut off its collector potential rises to ground. Simultaneously, due to the action of capacitor C19 the potential at the cathode of diode CR7 rises toward ground; however, before the potential reaches ground diode CR6 becomes forward biased and the cathode of CR7 is clamped at the fixed voltage source potential of −4.5 volts. Therefore, since the base potential of transistor Q15 is −10 volts when the transistor is saturated, diode CR7 is reverse-biased and capacitor C19 remains charged to −4.5 volts during the multivibrator stable state. As a result of the multivibrator action the signal at the collector of transistor Q15 has a negative-going edge delayed with respect to the positive-going edge of tape horizontal by an amount which is determined by the mode of color tape playback. During color tape playback in the normal color ATC mode the delay is 7.5 microseconds (figure 67E), and during playback in the non-phased color mode the delay is approximately 37 microseconds.

During the multivibrator stable state (i.e., transistor Q15 saturated), transistor Q17 is biased into saturation by current withdrawn from its base by the −10 volt potential at the collector of transistor Q15 via resistor R53, and the collector of Q17 is at ground potential. When transistor Q15 is cut off, a potential of +1 volt is applied to the base of transistor Q17 from the divider network consisting of resistors R54, R53, R47, and R48. This potential biases transistor Q17 into cut-off and its collector potential falls to approximately −17 volts. Thus transistor Q17 amplifies and inverts the output from the delay multivibrator, and the resulting signal appearing at its collector is fed via pin 30 of plug P1 to the linelock module (no. 316/B19) when the machine is playing back a color tape. If the machine is playing back a color tape in the normal color ATC mode, the output has a positive-going edge delayed by 7.5 microseconds with respect to tape horizontal (figure 67F). If the machine is playing back a color tape in the non-phased color mode, the output is delayed by approximately 37 microseconds with respect to tape horizontal (figure 67G).

Reference Horizontal Delay

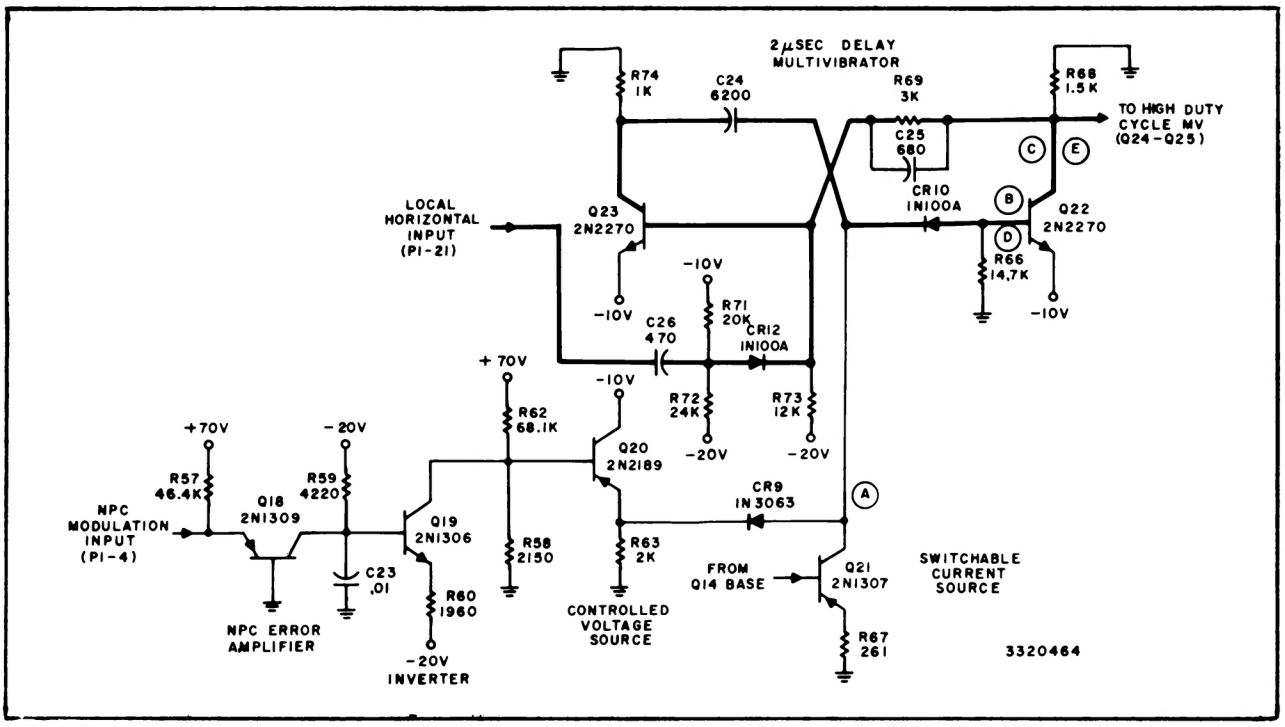
The purpose of the reference horizontal delay circuit, shown in figure 68, is to produce an output signal which is delayed with respect to reference horizontal by 2 microseconds when the machine is playing back a color tape in the normal color ATC mode and by nominally 30 microseconds when the machine is playing back a color tape in the non-phased color mode. The delay generated is equivalent to the timed cycle (unstable state) of a monostable multivibrator, and the multivibrator timed cycle is determined by the potential provided by a controlled voltage source in conjunction with current supplied by a switchable current source. The controlled voltage source potential is fixed at a value of approximately −4 volts during machine operation in the normal color ATC mode; however during non-phased color operation the voltage source potential is controlled by the THAF (tape horizontal alignment, fine) error signal. The switchable current source is controlled by the NPC bus potential, which is either −26 volts dc (when the ATC mode switch on the ATC delay/output module front panel is in COLOR ATC position) or ground (when the switch is in NON-PHASED COLOR position).

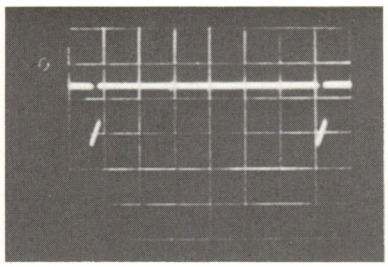
Reference horizontal fed to the module at pin 21 of plug P1 is obtained from the reference generator module (no. 312A/B18) and may be observed at test point TP2 (HOR) on the reference generator module front panel. The incoming reference horizontal is differentiated and the resulting positive-going spike, corresponding to the timed edge, drives monostable delay multivibrator Q22-Q23 into its timed cycle (unstable state) in exactly the same manner as tape horizontal drives delay multivibrator Q15-Q16 into its timed cycle. The operation of multivibrator Q22-Q23 is identical to that of multivibrator Q15-Q16 and, with the exception of the actual timing values, the circuit description of multivibrator Q15-Q16 presented above in the *Tape Horizontal Delay* discussion is also applicable to the circuit of multivibrator Q22-Q23. In the timing circuit of multivibrator Q22-Q23 the duration of the multivibrator timed cycle is determined by the potential provided by the controlled voltage source in conjunction with the magnitude of the charging current supplied. The controlled voltage source potential and charging current supplied are in turn controlled by the mode of color tape playback.

During color tape playback in the normal color ATC mode, NPC relay K31 is deenergized and pin 4 of plug P1 is essentially connected to an open circuit. Common base amplifier transistor Q18 is biased into conduction by current withdrawn from its base, and its collector current (approximately 1.5 milliamperes) establishes a collector potential of approximately −14 volts. This potential is applied directly to the base of inverter transistor Q19, and Q19 is thus biased into conduction by current flowing into its base. The collector current of transistor Q19 establishes a collector potential of approximately −4 volts, and this potential is in turn applied directly to the base of controlled voltage source transistor Q20. Transistor Q20, a PNP type, is biased into conduction by current withdrawn from its base by the −4 volt potential. Therefore, during machine operation in the normal color ATC mode the controlled voltage source potential appearing at the emitter of transistor Q20 has a fixed value of approximately −3.8 volts. Since diode CR9 is forward-biased when the multivibrator is in its stable state (as explained in the *Tape Horizontal Delay* circuit description above), the potential at the cathode of diode CR10 is approximately −3 volts and it is to this potential that capacitor C24 is clamped during the multivibrator stable state interval.

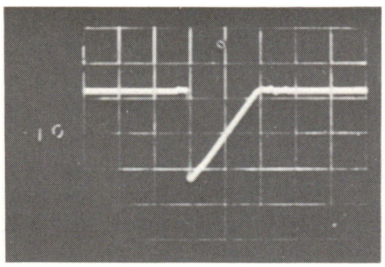
At the instant the multivibrator is driven into its unstable state (timed cycle) the potential across capacitor C24 falls to approximately −13 volts (figure 68A) and C24 begins to charge at a rate dependent upon the state of switchable current source transistor Q21 which in turn is controlled by the NPC bus potential. In the normal color ATC mode of color tape playback, the NPC bus potential is −26 volts dc and transistor Q21 is biased into conduction by current withdrawn from its base by a base potential of −3 volts which is developed as explained in the *Tape Horizontal Delay* circuit discussion above. Thus the charging current of capacitor C24 is the constant current provided by transistor Q21 plus the current flowing through resistor R66. The total charging current supplied, in conjunction with the fact that capacitor C24 begins to charge from −13 volts, allows C24 to charge to the saturation potential of transistor Q22 in 2 microseconds (figure 68B). Therefore, during color tape playback in the normal color ATC mode the delay multivibrator timed cycle is 2 microseconds, and the multivibrator output pulse is positive-going (figure 68C) with a leading edge timed to reference horizontal and a trailing edge delayed by 2 microseconds with respect to reference horizontal.

When the machine is playing back a color tape in the non-phased color mode the NPC bus potential is ground and switchable current source transistor Q21 is biased into cut-off as explained in the *Tape Horizontal Delay* circuit discussion above. In this case the

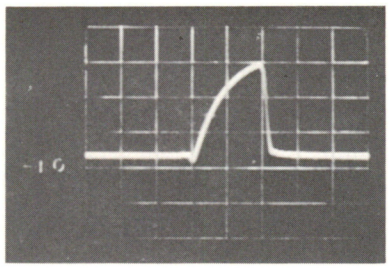




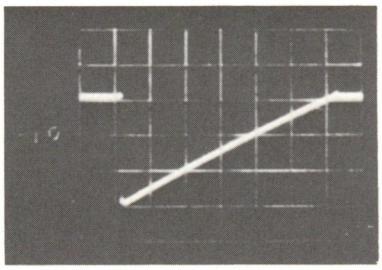
A. Q21 collector, 5v/cm.
(10 μsec/cm)



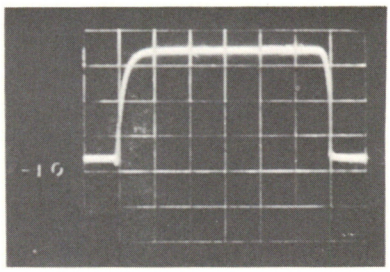
B. Q22 base, 1v/cm.
(1 μsec/cm)



C. Q22 collector, 2v/cm.
(1 μsec/cm)



D. Q22 base, 1v/cm.
NPC ground.
(5 μsec/cm)



E. Q22 collector, 2v/cm.
NPC ground.
(5 μsec/cm)

Machine in STOP mode (back-to-back signal).

Figure 68—Reference Horizontal Delay Circuit

charging current path of capacitor C24 is through resistor R66 and diode CR10 only and, with a steady controlled voltage source potential of −3 volts, the delay multivibrator timed cycle is lengthened to 30 microseconds. However, during non-phased color operation the controlled voltage source potential varies according to the THAF error signal generated in the color processor module. Since the level from which capacitor C24 begins to charge depends upon the controlled voltage source potential, any variation in the source potential will affect the time required by C24 to charge to the saturation potential of transistor Q22. Therefore, during non-phased color operation the delay multivibrator timed cycle varies according to the THAF error signal.

The THAF error signal is fed to the module at pin 4 of plug P1 from the color processor module via NPC relay K31 which is energized during tape playback in the non-phased color mode. The incoming error signal is a fluctuating current varying in amplitude over a maximum range of approximately ±1 milliampere. When the error signal current is zero, representing zero error, the current flowing through common base amplifier transistor Q18 is approximately 1.5 milliamperes as stated above in the discussion of circuit operation during playback in the normal color ATC mode. As the THAF error signal current increases in a positive direction the total current flowing through transistor Q18 increases and the collector potential of Q18 decreases (i.e., becomes less negative). Conversely, as the THAF error signal current increases in a negative direction the total current flowing through transistor Q18 decreases and the collector potential of Q18 increases (i.e., becomes more negative). The variation in potential at the collector of transistor Q18 is fed directly to the base of inverter transistor Q19 which is biased so that the maximum negative potential applied to its base cannot drive the transistor into cut-off, while at the same time the small positive potential obtained from the divider network consisting of resistors R58 and R62 in its collector circuit prevents the transistor from being driven into saturation by the maximum positive potential applied to its base. The varying potential appearing at the collector of transistor Q19 is inverted with respect to that fed to its base, thus the incoming THAF error signal has been converted from a varying current to a voltage which follows the current fluctuations directly. The varying potential at the collector of transistor Q19 is fed to the base of transistor Q20 and, since Q20 is biased into conduction by current withdrawn from its base, the potential appears at its emitter as the controlled voltage source potential.

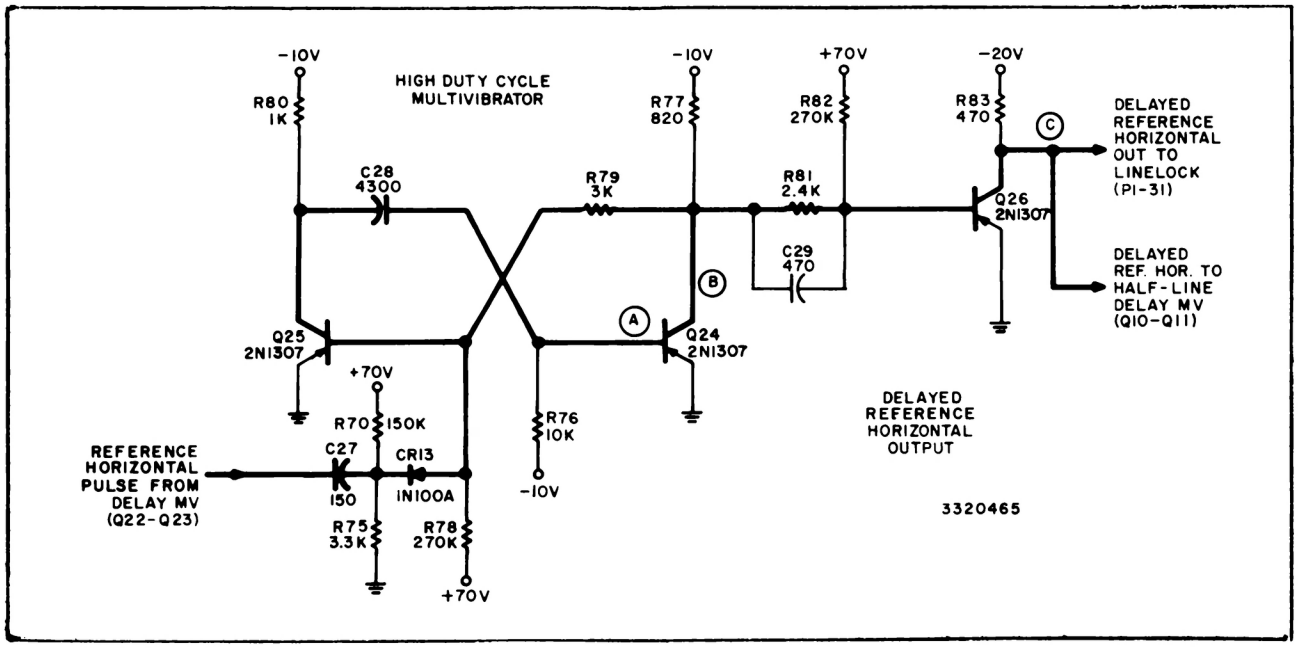
Since the negative potential from which capacitor C24 begins to charge at the start of the multivibrator timed cycle depends upon the controlled voltage source potential, during tape playback in the non-phased color mode the multivibrator timed cycle is modulated by the THAF error signal. When the THAF error signal is zero, the multivibrator timed cycle is 30 microseconds (figure 68D) and a positive-going 30 microsecond pulse appears at the collector of transistor Q22 (figure 68E). As the THAF error signal current increases in a positive direction the multivibrator timed cycle, and thus the width of the pulse at the collector of transistor Q22, increases. Conversely, as the THAF error signal increases in a negative direction the multivibrator time constant, and thus the width of the output pulse, decreases.

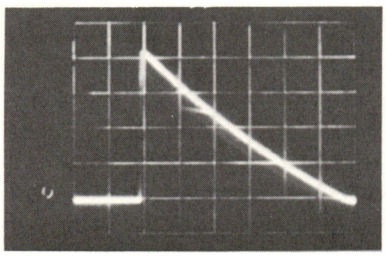
Therefore, during color tape playback in the non-phased color mode the delay of the delay multivibrator output pulse trailing edge, modulated by the THAF error signal, is 30 microseconds when the error signal is zero and may vary between the approximate limits of 10 and 50 microseconds as the THAF error signal varies from its most negative to its most positive value. During either normal color ATC or non-phased color playback, the pulse at the collector of transistor Q22 is fed to the high duty cycle multivibrator circuit.

High Duty Cycle Multivibrator and Delayed Reference Horizontal Output

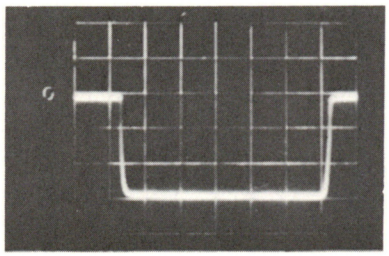
The high duty cycle multivibrator and delayed reference horizontal output circuits are shown in figure 69. The purpose of the high duty cycle multivibrator circuit is to increase the width of the delayed reference horizontal output pulse so that it may be more efficiently utilized in forming the reference trapezoid waveform in the linelock module. This is necessary primarily when playing back a color tape in the normal color ATC mode, since in this mode the 2 microsecond delay multivibrator output pulse is too narrow for proper generation of the linelock reference trapezoid waveform. The timed interval of the high duty cycle multivibrator is fixed at approximately 30 microseconds; therefore the width of the delayed horizontal output pulse is uniform regardless of whether the machine is operating in the normal color ATC mode with a delay multivibrator output pulse width of 2 microseconds or in the non-phased color mode where the delay multivibrator output pulse width varies according to the THAF error signal.

The input signal to the high duty cycle multivibrator is the output from the collector of transistor Q22 in the delay multivibrator circuit. The output

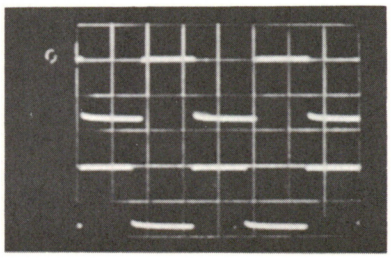




A. Q24 base, 2v/cm.
(5 μsec/cm)



B. Q24 collector, 2v/cm.
(5 μsec/cm)



C. Top: Q26 collector, 10v/cm.
COLOR ATC mode.
Bottom: Q26 collector, 10v/cm.
NPC mode.
(20 μsec/cm)

Machine in STOP mode (back-to-back signal).

Figure 69—High Duty Cycle Multivibrator and Delayed Reference Horizontal Output

signal is differentiated by the network consisting of capacitor C27 and resistors R70 and R75, and the resulting positive- and negative-going spikes appear at the cathode of diode CR13. Diode CR13 is normally reverse-biased and the positive-going spike appearing at its cathode has no effect on the diode. However the negative-going spike, corresponding to the trailing edge of the incoming pulse, forward biases the diode and is fed directly to the base of transistor Q25 as a triggering pulse.

Transistors Q24-Q25 and associated circuit components comprise the monostable high duty cycle multivibrator. In the multivibrator stable state transistor Q24 is saturated and transistor Q25 is cut off. In this condition the base and collector of transistor Q24 are at ground potential and the collector of transistor Q25 is at −10 volts. Capacitor C28 is then charged to 10 volts and the base potential of transistor Q24 is approximately 10 volts positive with respect to the collector potential of transistor Q25.

The negative-going triggering pulse fed to the base of transistor Q25 drives Q25 into saturation and its collector potential immediately rises to ground. Since the potential across capacitor C28 cannot change instantaneously, the base potential of transistor Q24 becomes approximately 8 volts positive with respect to ground. This potential biases transistor Q24 into cut-off and the multivibrator timed cycle (unstable state) begins.

At the instant transistor Q24 is driven into cut-off capacitor C28 begins to charge toward −10 volts through resistor R76. When capacitor C28 has charged to a potential which is slightly negative with respect to ground, transistor Q24 is biased into saturation once again and its collector potential immediately rises to ground. A positive potential of approximately +0.8 volt is then applied to the base of transistor Q25 from the divider network consisting of resistors R78 and R79 connected between the +70 volt bus and ground. The positive potential biases transistor Q25 into cut-off and the multivibrator timed cycle ends.

The duration of the multivibrator timed cycle is equivalent to the time required by capacitor C28 to charge from +8 volts to the saturation potential of transistor Q24, and the values of C28 and resistor R76 are such that the timed cycle is 30 microseconds (figure 69A). As a result of the multivibrator action the signal at the collector of transistor Q24 is a negative-going pulse having a width of 30 microseconds (figure 69B) and a leading edge timed to the trailing edge of the delay multivibrator output pulse.

During the high duty cycle multivibrator stable state interval the collector potential of transistor Q24 is ground and a positive potential of approximately +0.6 volt is applied to the base of delayed reference horizontal output transistor Q26 from the divider network consisting of resistors R81 and R82. This potential biases transistor Q26 into cut-off and its collector potential is approximately −18 volts. When the high duty cycle multivibrator is triggered into its unstable state, transistor Q26 is driven into saturation by current withdrawn from its base by the negative potential appearing at the collector of transistor Q24 and its collector potential rises to ground. Thus output transistor Q26 amplifies and inverts the 30 microsecond pulse developed by the high duty cycle multivibrator.

When the machine is playing back a color tape in the normal color ATC mode, the positive-going output pulse at the collector of transistor Q26 has a width of 30 microseconds (figure 69C, top) and a positive-going leading edge delayed by 2 microseconds with respect to reference horizontal. (See timing diagram, figure 70.) When the machine is playing back a color tape in the non-phased color mode the positive-going pulse at the collector of transistor Q26 has a width of 30 microseconds (figure 69C, bottom) and a positive-going leading edge delayed with respect to reference horizontal by an amount dependent upon the THAF error signal. With a THAF error signal of zero, the leading edge of the output pulse is delayed by 30 microseconds with respect to reference horizontal. As the THAF error signal varies from its most negative to its most positive value, the delay varies from 10 to 50 microseconds.

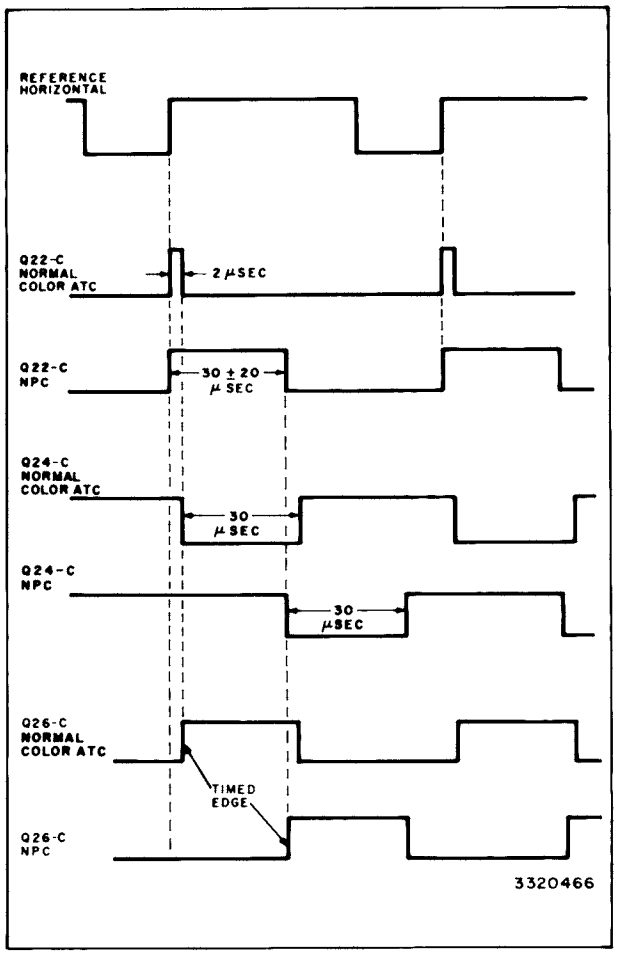
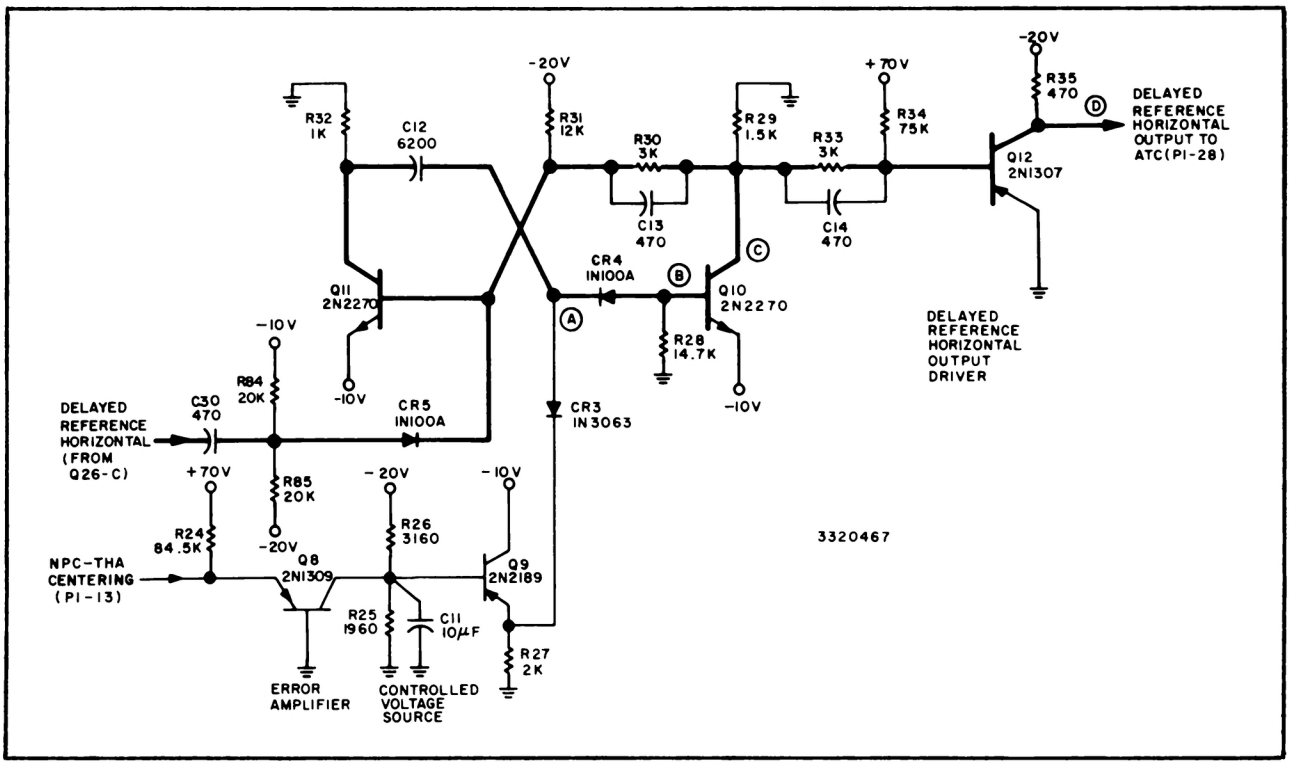
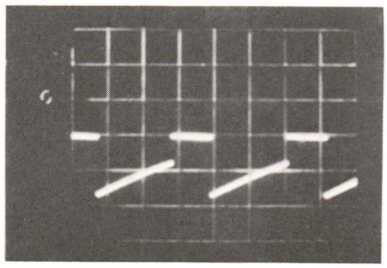


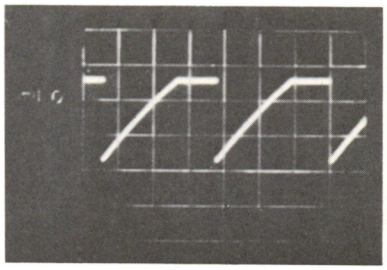
Figure 70—High Duty Cycle Multivibrator Timing Diagram

The positive-going delayed reference horizontal pulse appearing at the collector of transistor Q26 is fed to the half-line delay multivibrator circuit described below and, via pin 31 of plug P1, to the linelock module (no. 316/B19) where it is utilized in generating the linelock trapezoid waveform.

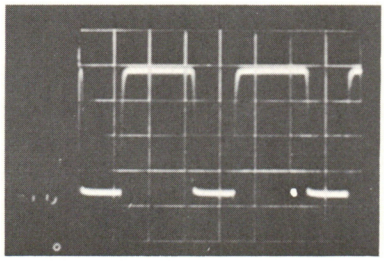




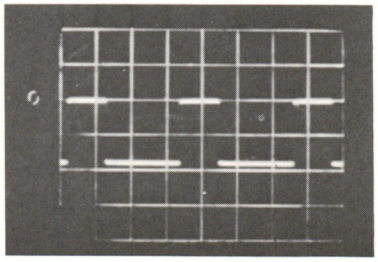
A. CR4 cathode, 5v/cm.



B. Q10 base, 2v/cm.



C. Q10 collector, 2v/cm.



D. Q12 collector, 10v/cm.

Machine in STOP mode (back-to-back signal). All sweep times 20 μsec/cm.

Figure 71—Half-Line Delay Multivibrator and Horizontal Output Circuits

Half-Line Delay Multivibrator

The half-line delay multivibrator circuit (figure 71) functions during color tape playback in both the normal color ATC and non-phased color modes, however the delayed reference horizontal output pulse from the multivibrator is utilized by the ATC system only during non-phased color playback. The following discussion, therefore, pertains to circuit operation during playback in the non-phased color mode only.

The purpose of the half-line delay multivibrator is to provide a delay of approximately one-half a TV line so that when combined with the delay provided by the 2 microsecond delay multivibrator (30 microsecond delay in the non-phased color mode) a total delay of approximately one TV line (63.5 microseconds) is attained. A delay of one TV line provides approximate alignment of the delayed reference horizontal pulse with undelayed tape horizontal fed to the monochrome ATC system. Thus the ATC sample pulse, derived from tape horizontal, will sample on the slope of the ATC trapezoid waveform developed from delayed reference horizontal. The actual delay provided by the half-line delay multivibrator is controlled by the THA (tape horizontal alignment) error signal developed in the monochrome ATC system. The THA error signal may be considered a measure of the phase difference between tape and reference horizontal; therefore, the THA error signal controls the multivibrator delay so that, on the average, the monochrome ATC sample pulse will sample precisely at the center of the reference trapezoid slope.

The signal appearing at the collector of output transistor Q26 in the high duty cycle multivibrator circuit is differentiated by the network consisting of capacitor C30 and resistors R84 and R85, and the resulting positive- and negative-going spikes appear at the anode of diode CR5 (figure 71). During normal stable state conditions diode CR5 is reverse-biased and the negative-going spike appearing at its anode has no effect on the diode. However the positive-going spike, corresponding to the delayed edge, forward biases the diode and is fed to the base of transistor Q11 as a triggering pulse.

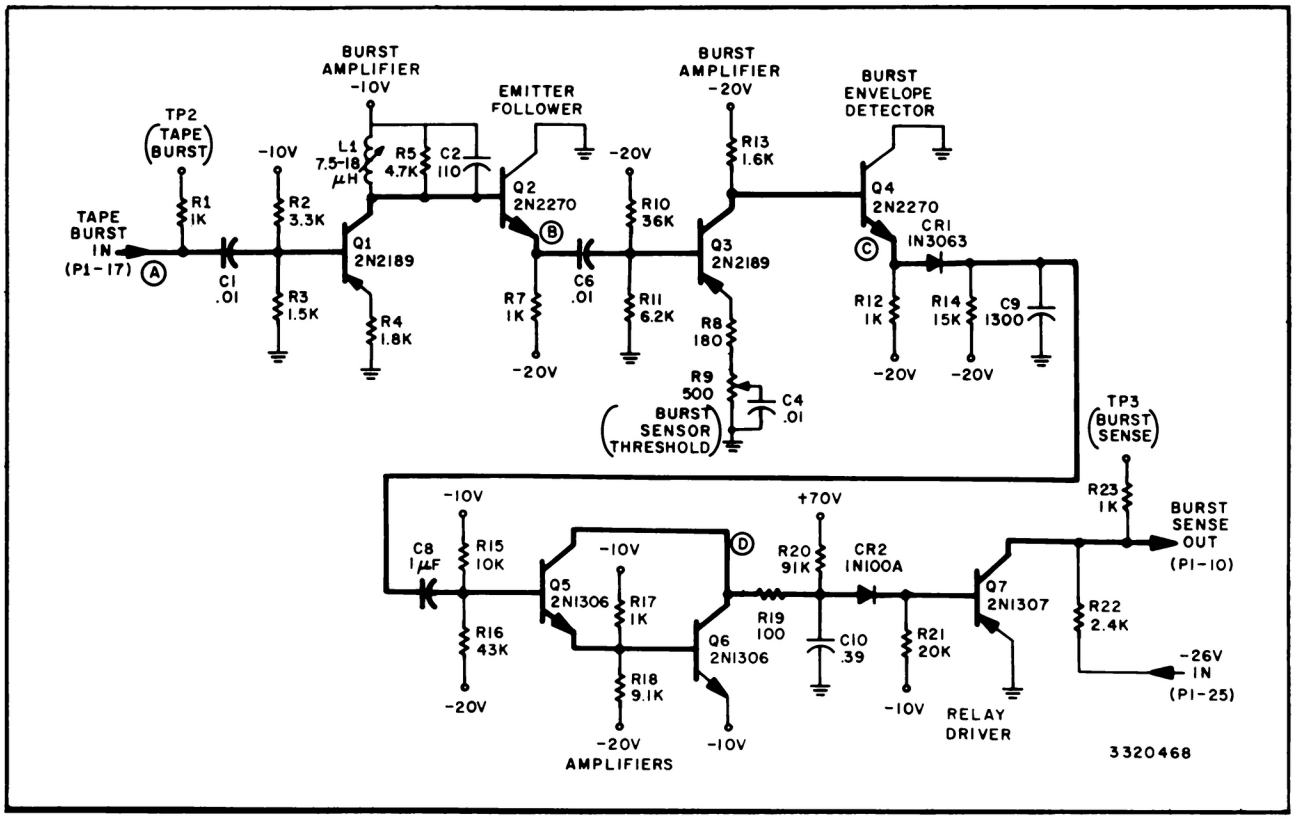
Transistors Q10-Q11 and associated circuit components form the monostable half-line delay multivibrator. In the multivibrator stable state transistor Q10 is saturated and transistor Q11 is cut off; thus the base and collector potential of transistor Q10 are approximately −10 volts and the collector of transistor Q11 is at ground potential. Capacitor C12 is charged to the controlled voltage source potential (nominally −5 volts); therefore the potential at the cathode of diode CR4 is approximately −5 volts and the diode is reverse-biased.

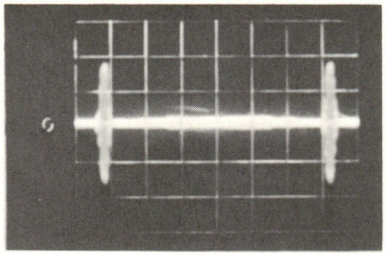
The positive-going triggering pulse fed to the base of transistor Q11 drives Q11 into saturation and its collector potential immediately falls to approximately −9 volts. Since the potential across capacitor C12 cannot change instantaneously, the potential at the cathode of diode CR4 remains −5 volts with respect to the collector potential of transistor Q11 and is therefore −14 volts with respect to ground. Diode CR4 is thereby forward-biased and a potential of approximately +13 volts appears at the base of transistor Q10. This potential biases transistor Q10 into cut-off and the multivibrator timed cycle (unstable state) begins.

At the instant transistor Q10 is biased into cut-off, capacitor C12 begins to charge toward ground through forward-biased diode CR4 and resistor R28. When capacitor C12 has charged to a potential which is slightly positive with respect to −10 volts, transistor Q10 is biased into saturation once again and the multivibrator timed cycle ends. Diode CR4 is then reverse-biased and transistor Q11 is biased into cut-off by a potential of approximately −12 volts applied to its base from the divider network consisting of resistors R31 and R30 connected between the −20 volt bus and the negative potential at the collector of transistor Q10. When transistor Q11 is biased into cut-off its collector potential immediately rises to ground and, due to the action of capacitor C12, the cathode potential of diode CR4 rises sharply to the controlled voltage source potential (figure 71A).

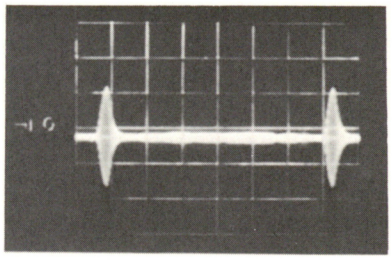
The timed cycle of the half-line delay multivibrator is equivalent to the time required by capacitor C12 to charge to the saturation potential of transistor Q10. Thus the multivibrator timed cycle is determined by the values of capacitor C12 and resistor R28 in conjunction with the potential from which C12 begins to charge at the start of the cycle. The potential from which capacitor C12 begins to charge depends upon the voltage source potential which in turn is controlled by the THA error signal.

The THA error signal is fed to the module at pin 13 of plug P1 from the ATC error detector module (no. 225/B13) via NPC relay K32 which is energized when the machine is playing back a color tape in the non-phased color mode. The incoming error signal is a varying current having an approximate range of 0.5 to 2.5 milliamperes and a nominal value of 1.5 milliamperes which corresponds to zero error.

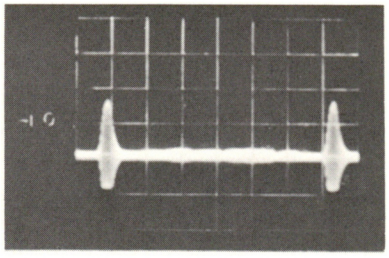




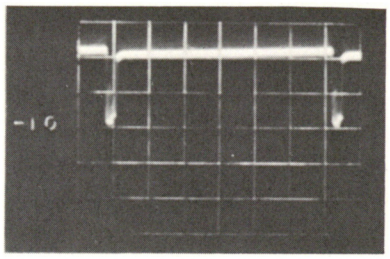
A. Tape burst (P1-17), 1v/cm.



B. Q2 emitter, 2v/cm.



C. Q4 emitter, 5v/cm.



D. Q6 collector, 1v/cm.

Machine in STOP mode (back-to-back signal). All sweep times 10 μsec/cm.

Figure 72—Burst Sensor

The error signal is fed directly to the emitter of common base amplifier transistor Q8, which is biased into conduction by current withdrawn from its base. With no input error signal, a current of approximately 0.8 milliampere flows through transistor Q8. The incoming error signal current adds to this value; therefore the total collector current of transistor Q8 depends upon the magnitude of the error signal current.

When the THA error is zero (i.e., the incoming error signal current is 1.5 milliamperes) the collector current of transistor Q8 is 2.3 milliamperes and its collector potential is approximately −5.5 volts. This potential is applied directly to the base of controlled voltage source transistor Q9. Transistor Q9 is then biased into conduction by current withdrawn from its base, and the −5.5 volt potential appears at its emitter as the controlled voltage source potential. As the THA error signal current increases, the collector potential of transistor Q8, and thus the controlled voltage source potential, decreases (i.e., becomes less negative). Conversely, as the THA error signal current decreases, the controlled voltage source potential increases (i.e., becomes more negative). The half-line delay multivibrator timed cycle is directly proportional to the negative controlled voltage source potential; therefore as the THA error signal decreases, the multivibrator timed cycle increases, and vice versa. The nominal controlled voltage source potential of approximately −5 volts results in a multivibrator timed cycle of approximately 35 microseconds (figure 71B). During the multivibrator timed cycle diode CR3 is reverse-biased and the controlled voltage source is isolated from the multivibrator timing circuit.

As a result of the multivibrator action a positive-going pulse appears at the collector of transistor Q10 (figure 71C). The width of this pulse is equal to the half-line delay multivibrator timed cycle, and when the THA error is zero the pulse has a width of approximately 35 microseconds. During the multivibrator stable state, output driver transistor Q12 is biased into saturation by current withdrawn from its base by the negative potential at the collector of transistor Q10. When the multivibrator begins its timed cycle and transistor Q10 is cut off, a potential of +1 volt is applied to the base of transistor Q12 from the divider network consisting of resistors R34, R33, R29 and R30. This potential biases transistor Q12 into cut-off and its collector potential falls to approximately −18 volts. Thus output driver transistor Q12 amplifies and inverts the half-line delay multivibrator output, and the signal appearing at its collector (figure 71D) has a positive-going edge which is delayed by approximately one TV line with respect to reference horizontal.

The delayed reference horizontal output from transistor Q12 is fed via pin 28 of plug P1 to a normally open contact of NPC relay K31. When the machine is playing back a color tape in the non-phased color mode relay K31 is energized and delayed reference horizontal is fed to the monochrome ATC reference module (no. 226/B14) where it is utilized in generating the ATC trapezoid waveform.

Burst Sensor

The purpose of the burst sensor circuit is to detect the presence of tape burst and to develop a burst sense signal which controls the error clamp circuit in the color error detector module and the regenerated burst circuit in the color processor module. In brief, when the machine is playing back a color tape containing a normal burst signal, the burst sensor circuit develops a burst sense signal which disables the error clamp circuit and allows the regenerated burst circuit to function. Conversely, if for any reason tape burst does not exist, the burst sense signal provided by the burst sensor circuit enables the error clamp circuit, kills regenerated burst, and disables the THAF reset clamp circuit in the color processor module.

Tape burst, separated from the tape chroma signal in the chroma separator module (no. 325/C13), is fed to the module at pin 17 of plug P1 and may be observed at test point TP2 (TAPE BURST). The incoming signal (figure 72A) is coupled to the base of amplifier transistor Q1 which is biased into conduction by the negative potential at the junction of resistors R2 and R3. Variable inductor L1, capacitor C2, and resistor R5, in the collector circuit of transistor Q1 form a parallel network which is tuned to the subcarrier frequency, and the amplified tape burst signal appearing at the collector of Q1 is fed directly to the base of emitter follower transistor Q2. Transistor Q2 isolates the tuned network from the amplification circuit which follows, and the tape burst signal appearing at its emitter (figure 72B) is coupled to the base of transistor Q3. Transistor Q3, biased into conduction by the negative potential at the junction of resistors R10 and R11, further amplifies the tape burst signal, and the amplified signal appearing at its collector is fed directly to the base of burst envelope detector transistor Q4. The gain of transistor Q3 may be varied over a small range by adjusting potentiometer R9 (BURST SENSOR THRESHOLD), and the potentiometer is nominally set so that an incoming tape burst signal amplitude of one volt peak-to-peak will be sufficient to cause relay

driver transistor Q7 to saturate and thus disable the error clamp circuit in the color error detector module. The proper procedure for adjusting potentiometer R9 is presented under *Adjustments* at the end of the module circuit description.

During the interval between tape burst signals the d-c potential at the collector of transistor Q3, and thus at the base of transistor Q4, is approximately −14 volts. Transistor Q4 is then biased into conduction, essentially by current withdrawn from its emitter by the −20 volt supply via resistor R12, and its emitter potential is also approximately −14 volts. Therefore, during the interval between tape burst signals, diode CR1 is forward-biased and capacitor C9 charges to approximately −14 volts. When the tape burst signal appears at the emitter of transistor Q4 (figure 72C) the negative-going portion of the signal cuts off diode CR1, thus only the positive-going portion of the signal passes through the diode to capacitor C9. Capacitor C9 presents a low impedance to the subcarrier frequency component of the positive-going portion of the signal and thereby bypasses this component to ground. The resulting envelope is essentially a positive-going pulse which occurs at the line rate and is timed to the tape burst interval.

The positive-going pulse is coupled to the amplifier circuit consisting of transistors Q5-Q6 and associated circuit components. The d-c potential applied to the base of transistor Q5 is approximately −12 volts, as determined by the divider network consisting of resistors R15 and R16 connected between the −10 and −20 volt supplies. Also, the d-c potential applied to the base of transistor Q6 from the divider network consisting of resistors R17 and R18 is approximately −11 volts dc. These potentials are such that transistors Q5 and Q6 are normally biased into cut-off. When the positive-going burst envelope pulse is fed to the base of transistor Q5 the transistor is driven into conduction and a corresponding positive-going pulse appears at its emitter. Since the emitter of transistor Q5 is connected directly to the base of transistor Q6 (figure 72), the positive-going pulse at the emitter of Q5 drives Q6 into saturation and the collector potential of Q6 goes to −10 volts (figure 72D).

Transistor Q6 is thus in effect driven into saturation by the positive-going burst envelope pulse, and when the first pulse appears capacitor C10 rapidly charges toward −10 volts through Q6 and resistor R19. This results in a negative potential at the anode of diode CR2, and the negative potential allows relay driver transistor Q7 to become saturated by current withdrawn from its base by the −10 volt supply via resistor R21. When transistor Q7 is saturated its base is at ground potential and, since the cathode of diode CR2 is also then at ground potential, CR2 is reverse-biased. After the positive-going burst envelope pulse has occurred, transistors Q5 and Q6 are returned to their normal cut-off condition and capacitor C10 begins to discharge slowly through resistor R20 toward +70 volts. Since the R20-C10 time constant is large, capacitor C10 cannot discharge more than a few tenths of a volt before the next burst envelope pulse appears and causes C10 to charge once again toward −10 volts. Therefore, after the first few burst envelope pulses have occurred capacitor C10 becomes fully charged to a potential of approximately −8 volts and maintains diode CR2 in a cut-off state during the entire TV line. Transistor Q7 thus remains saturated during the entire TV line and an uninterrupted ground potential appears at its collector. The ground potential is fed from pin 10 of plug P1 to the color error detector module (no. 326/C14), via the color processor module (no. 231/C15), where it disables the color error clamp circuit and allows the regenerated burst circuit to function, as explained in the appropriate module circuit description.

If the tape burst signal is not present for any reason, there will be no burst envelope pulse and transistors Q5 and Q6 will remain cut off. In this case diode CR2 will be forward-biased and a potential of approximately +4 volts will be applied to the base of transistor Q7 from the divider network consisting of resistors R20 and R21 connected between the +70 and −10 volt supplies. The positive potential biases transistor Q7 into cut-off and ground potential is removed from its collector. The burst sense signal appearing at pin 10 of plug P1 is then approximately −23 volts dc, as determined by the network consisting of resistor R22 and other resistors in the logic circuits which it controls. The burst sense potential may be observed at test point TP3 (BURST SENSE).

Adjustments

The following color sensor module adjustment procedures are part of the system setup adjustments, and once set should not normally require re-adjustment. Test equipment required when making the adjustments consists of a dual-trace oscilloscope such as the *Tektronix Type 535-A* or the equivalent.

Inductor L1

1. Place the color sensor module on a module extender.

2a. In TR-22 machines rotate the FM standards switch (module no. 205) to COLOR STD 1 or 2 position; in TR-3 machines rotate the demodulator output switch (module no. A18) to COLOR position; in TR-4 machines rotate both the demodulator output switch and the modulator switch (module nos. A18 and A2) to COLOR position.

b. In all machines rotate the ATC mode selector switch on the ATC delay/output module (no. 223/B11) to COLOR ATC position.

3. In TR-22 and TR-4 machines feed a color bar signal (split field with 100% white bar), 3.58 mc subcarrier (4.43 mc subcarrier if machine is operated on 625-line standards), and sync to the machine, and operate the machine in STOP mode (MOD-DEMOD). In TR-3 machines, remove the ATC video out pins (nos. 14 and 30) from the demodulator output module receptacle at the rear of the machine; feed a 1 volt peak-to-peak color signal, subcarrier, and sync to the machine; and operate the machine in STOP mode.

4. Connect the external oscilloscope probe to the emitter of transistor Q2, and set up the oscilloscope sweep for a horizontal rate presentation.

5. Tune inductor L1 for maximum burst amplitude.

7.5 Microsecond Delay

1. Set up machine for operation in the STOP mode according to steps 1, 2, and 3 in the *Inductor L1* tuning procedure above.

2. Connect external oscilloscope probe to the collector of transistor Q15.

3. Adjust potentiometer R44 (DELAY ADJ) for a pulse width of 7.5 microseconds, as observed on the oscilloscope.

Burst Sensor Threshold

1. Set up machine according to steps 1 and 2 in the *Inductor L1* tuning procedure above.

2. Play back a tape containing color information and adjust the FM EQ control on the FM equalizer module (no. 132/A21) front panel for a 1 volt peak-to-peak burst signal at test point TP2 (TAPE BURST).

3. Connect the external oscilloscope probe to the collector of transistor Q7, with the oscilloscope sweep set for a vertical rate presentation and with the oscilloscope input on DC.

4. Adjust potentiometer R9 (BURST SENSOR THRESHOLD) so that transistor Q7 just begins to conduct (i.e., the collector potential rises from −26 volts dc to ground). Then adjust the potentiometer one full turn in the clockwise direction.

INSTALLATION

All wiring required by the color ATC system is contained in the monochrome ATC harness; therefore the monochrome ATC system must be properly installed before the color ATC system can be installed. (TR-22 machines having serial numbers above no. 1300 have the monochrome ATC wiring, and thus the color ATC wiring, included as a standard part of the machine.) In addition, the installation procedures presented in this section for both TR-22 and TR-3/TR-4 machines assume that the monochrome ATC system has been modified for the NPC (non-phased color) mode of operation.

INSTALLATION IN TR-22 MACHINES

Color ATC System

The following procedure is recommended for the installation of the ES-43581 color ATC system in TR-22 Television Tape Recorders. (Instructions for installing the MI-40693 early model color ATC systems are contained in the preliminary color ATC instruction book, IB-31652-P.) Items referred to in the installation procedure pertain to items contained in MI-43353 and MI-40688, and are described in table III.

1. Remove the blank front panels covering module apertures 231 and 232, and 323 through 326, in the following manner:

a. Remove one or two modules adjacent to both sides of the blank panels.

b. Loosen the two nuts in the back of each blank panel with a 5/16-inch open end wrench until the clamps held by the nuts can be rotated 180 degrees.

c. Lift the blank panels up and pull out.

2. Install the color fixed delay line assembly (item 1 of MI-40688) by one of the two procedures outlined below, depending upon the machine serial number.

TABLE III. INSTALLATION ITEMS PROVIDED WITH COLOR ATC SYSTEM (ES-43581 and ES-43582)

Item No.			*Description*
MI-43353	*MI-40688*	*MI-43392*	
1			Module, Color Processor (no. 231/C15)
2			Module, Color Phase (no. 232/C16)
3			Module, Color Sensor (no. 323/C11)
4			Module, Color Delay (no. 324/C12)
5			Module, Chroma Separator (no. 325/C13)
6			Module, Color Error Detector (no. 326/C14)
	1		Fixed Delay Line Assembly (Mono/Color ATC)
	2		3 Brackets (TR-22A, B only)
	3		Support
	4		Resistor, 820-ohm, ½-watt, 5% (TR-22A, B only)
	5		Angle
	6		2 Mounting Lugs (TR-22C only)
	7		Hardware: 12 Screws, #8-32 x .44 9 Flat Washers, #8 1 Nut, #8-32 10 Lockwashers, #8
		1	Module, ATC Fixed Delay Line (no. 3A3)

Serial numbers below no. 1301:

a. Disconnect the two coax cables at FDL2-J1 and FDL2-J2 on the connector bracket which is fastened to the monochrome ATC fixed delay line assembly at the rear of the machine.

b. Remove the connector bracket and discard.

c. Fasten the three mounting brackets (item 2) to the bottom of the fixed delay line assembly utilizing screws, flat washers, and lock washers provided (item 7). (Refer to figure 73.)

d. Fasten the angle (item 5) to the center mounting bracket (directly beneath J2) installed in step c above, utilizing the front screw which holds the bracket to the delay line box. (The right angle should be approximately flush with the front edge of the box, as shown in figure 73.)

e. Fasten the color fixed delay line to the monochrome fixed delay line, utilizing the hardware supplied (item 7), by inserting a screw, with a lock washer, through each of the color fixed delay line mounting brackets and into the tapped holes of the monochrome fixed delay line mounting brackets.

f. Fasten the vertical support (item 3) to the color fixed delay line by attaching the upper end (straight end) to the angle (mounted in step d above) utilizing a screw, nut, flat washer, and lock washer (item 7). Fasten the lower end of the support to the base of the machine by first loosening the right-hand screw holding resistors 11R2 and 11R3, and then slipping the slotted leg of the support under the screw head. Re-tighten the screw.

g. Connect the coax cables to FDL2-J1 and FDL2-J2.

Serial numbers above no. 1300:

a. Disconnect the two coax cables designated FDL2-J1 and FDL2-J2 from the connectors which are mounted on the ATC fixed delay line plate at the rear of the machine, and remove the connectors from the plate.

b. Fasten the two mounting lugs (item 6 of MI-40688) to the bottom of the color fixed delay line box, utilizing the hardware supplied (item 7), by inserting screws, with flat washers, into the threaded holes at each end of the box. (The mounting lugs must extend beyond the ends of the delay line box.)

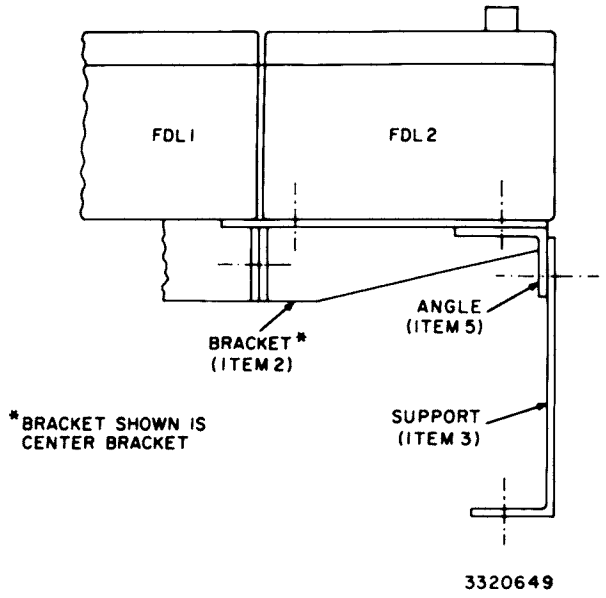


Figure 73—Center Bracket and Support Assembly Utilized in Mounting Color Fixed Delay Line in TR-22 Machines

c. Fasten the color fixed delay line to the plate holding the monochrome fixed delay line by inserting screws, with flat washers, (item 7) through the mounting lugs and into the tapped holes in the plate.

d. Connect the coax cables to FDL2-J1 and FDL2-J2.

3. In machines bearing serial numbers below no. 1301, modify the sync logic module (no. 230) circuitry by replacing resistor R4 (1800 ohms) with an 820 ohm, ½ watt, 5% resistor (item 4).

4. Remove the following wires by clipping with diagonal cutters at each end near the tapered pins of the receptacle:

From pin 8 of module no. 231 to pin 24 of module no. 232.

From pin 8 of module no. 323 to pin 24 of module no. 326.

5. Check the d-c voltage inputs to each color ATC module by inserting a module extender into the module receptacle and measuring the voltages at pins 7, 9, 22, and 25. The voltages measured should be as follows:

Pin 7	−20V
Pin 9	−10V
Pin 22	+70V
Pin 25	−26V

6. Insert the color ATC system modules (items 1 through 6 of MI-43353) into their proper receptacles.

Remote SYSTEM PHASE and BURST PHASE Controls

Provision is made for remote as well as local control of the system subcarrier and burst subcarrier phasing in the color ATC system. Two procedures for installing the controls in remote locations are presented below. The first procedure outlines a method of installing the controls in the MI-40692 video remote control panel. (This procedure assumes that the video remote control panel has been installed correctly and that its other functions are operating properly.) The second procedure outlines a method of installing the controls in a separate remote control panel.

Installation in the MI-40692 Video Remote Control Panel

1. Cut the jumper connecting pins 3 and 4 of the SIGNAL REMOTE connector J26 which is mounted on the connector plate in the lower section of the machine. (Machines bearing serial numbers above no. 1300 will not have this jumper.)

2. Make certain the remote light ground wire is connected to pin 4 of J26. (If it is connected to pin 3 it must be moved to pin 4.)

3. In machines bearing serial numbers below no. 1301, connect a wire between pin 3 of J26 and position 11 of the color phase module (no. 232) receptacle, utilizing a spare taper pin.

4. In the color phase module circuitry remove the jumper which connects the center-arm of the SYSTEM PHASE control (potentiometer R2) to the junction of resistors R7 and R8.

> NOTE: When the jumper has been removed, the SYSTEM PHASE control may be operated only from the remote location (regardless of the mode of the LOCAL/REMOTE switch on the RECORD control panel) unless step 5 below is carried out.

5. If it is desired to operate the SYSTEM PHASE control similarly to the BURST PHASE control, i.e. either locally (at the color phase module front panel) or remotely, make the following modifications in the color phase module circuitry:

a. At the junction of resistors R7 and R8, unsolder the wire which runs to pin 11 of plug P1. Solder the wire to the unused normally open contact of relay K1.

b. At the junction of resistors R7 and R8, unsolder the wire which runs to the center-arm of the SYSTEM PHASE control (potentiometer R2). Solder the wire to the unused normally closed contact of relay K1.

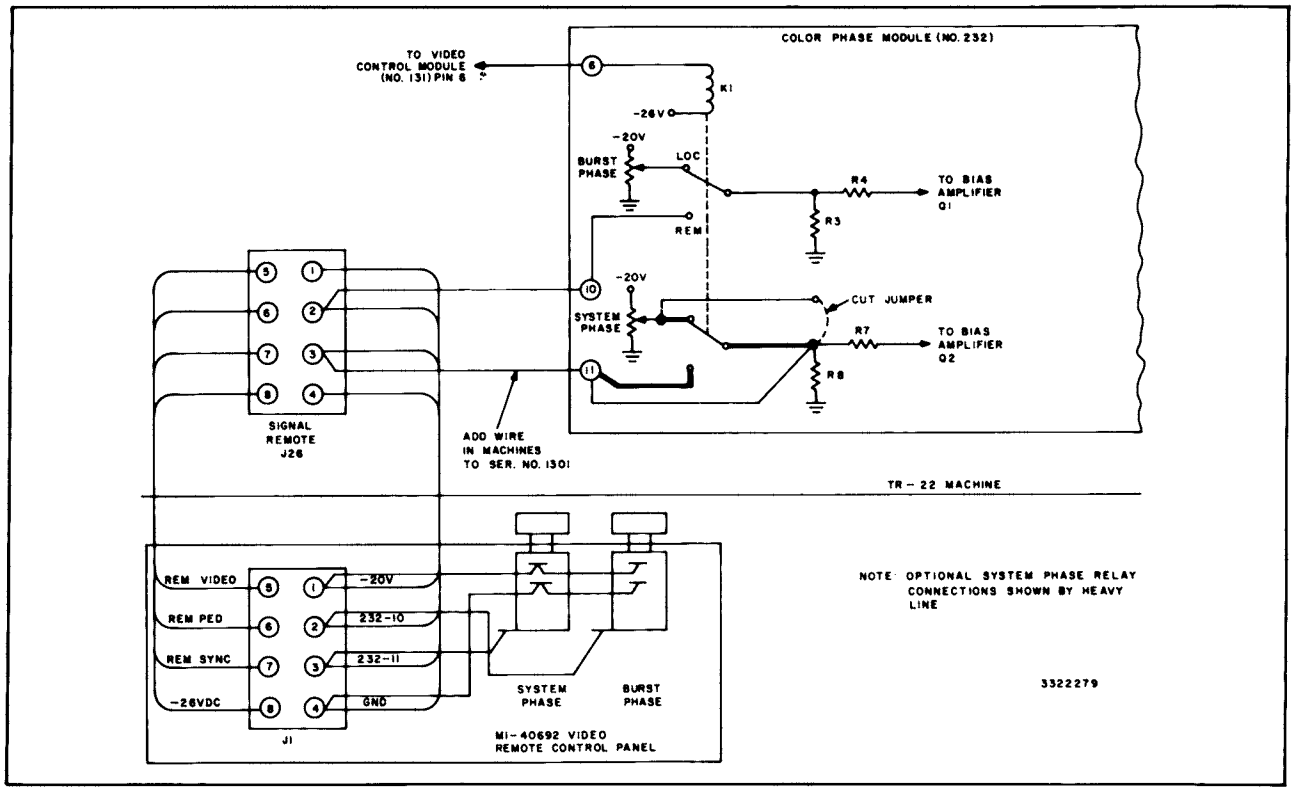


Figure 74—Installation of Burst and System Phase Controls in MI-40692 Video Remote Control Panel (TR-22 Machines)

c. Solder a wire between the junction of resistors R7 and R8 and the unused common contact of relay K1. (See figure 74.)

6. Solder a wire to pin 6 of the video control module (no. 131) receptacle, run the wire with the existing cabling to the receptacle of module no. 232, solder to a spare taper pin, and insert the pin in position 6. (This step allows the LOCAL/REMOTE pushbutton switch on the RECORD control panel to be utilized in delegating control of burst and system phasing to the local or remote location.)

7. Mount two 10K ohm *Bournes* potentiometers (RCA drawing no. 8546679-105; stock no. 230513) on the MI-40692 video remote control panel. Label one potentiometer SYSTEM PHASE and the other potentiometer BURST PHASE.

8. Unsolder the wire connected to pin 3 of jack J1 on the remote control panel and solder it to pin 4, so that there are now two wires soldered to pin 4.

9. Solder a jumper between the terminal closest to the shaft of the SYSTEM PHASE potentiometer and the terminal closest to the shaft of the BURST PHASE potentiometer, and solder a wire from this jumper to the −20 volt bus of the remote control panel. (−20 volts dc is fed to the remote control panel at pin 1 of jack J1.)

10. Solder a jumper between the center terminal of the SYSTEM PHASE potentiometer and the center terminal of the BURST PHASE potentiometer, and solder a wire from this jumper to the ground bus of the remote control panel. (Ground potential is applied to the remote control panel at pin 4 of jack J1.)

11. Solder a wire between the center-arm (slider) of the SYSTEM PHASE potentiometer and pin 3 of jack J1.

12. Solder a wire between the center-arm (slider) of the BURST PHASE potentiometer and pin 2 of jack J1.

13. Add wires to the existing remote control cable which will connect pin 2 of J26 (at the machine) to pin 2 of J1 (at the remote control panel) and pin 3 of J26 to pin 3 of J1.

Installation in a Separate Remote Control Panel

1. Cut the jumper connecting pins 3 and 4 of the SIGNAL REMOTE connector J26 which is mounted on the connector plate in the lower section of the machine. (Machines bearing serial numbers above no. 1300 will not have this jumper.)

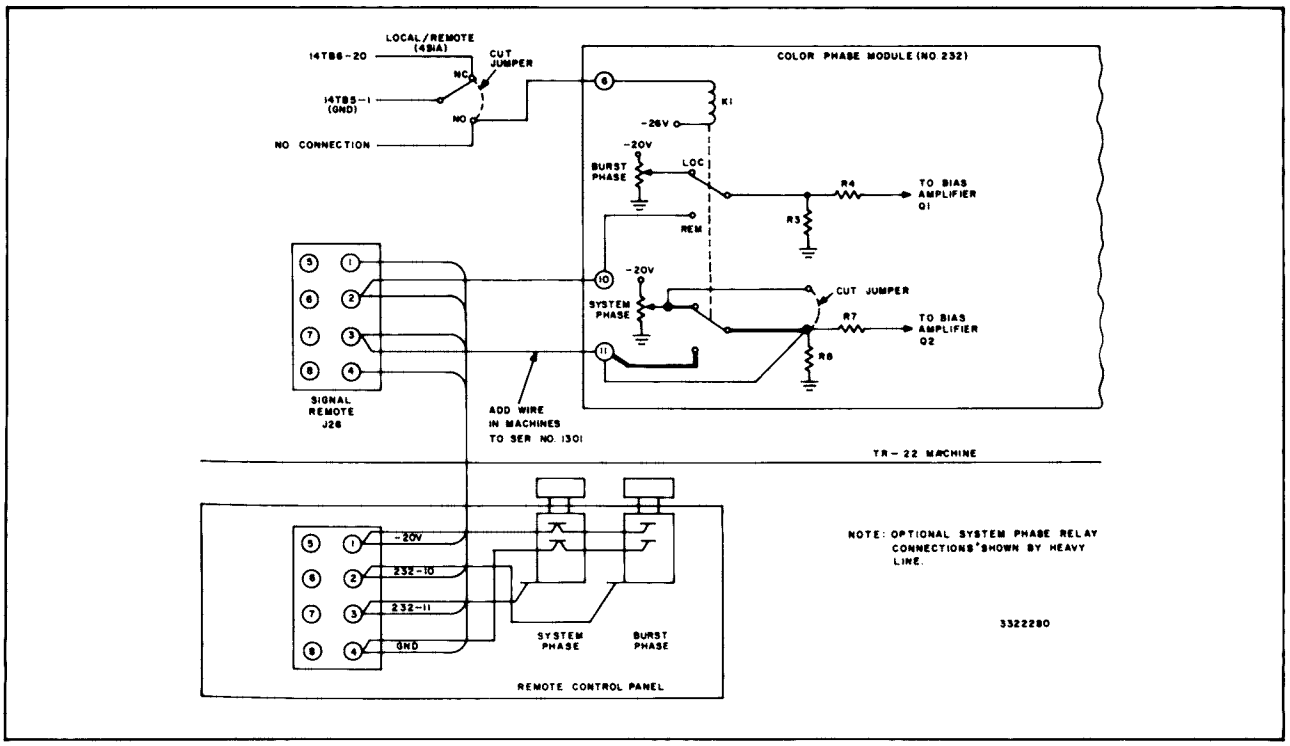


Figure 75—Installation of Burst and System Phase Controls in Separate Remote Control Panel (TR-22 Machines)

2. Make certain the remote light ground wire is connected to pin 4 of J26. (If it is connected to pin 3 it must be moved to pin 4.)

3. In machines bearing serial numbers below no. 1301, connect a wire between pin 3 of J26 and position 11 of the color phase module (no. 232) receptacle, utilizing a spare taper pin.

4. In the color phase module circuitry remove the jumper which connects the center-arm of the SYSTEM PHASE control (potentiometer R2) to the junction of resistors R7 and R8.

> NOTE: When the jumper has been removed, the SYSTEM PHASE control may be operated only from the remote location (regardless of the mode of the LOCAL/REMOTE switch on the RECORD control panel) unless step 5 below is carried out.

5. If it is desired to operate the SYSTEM PHASE control similarly to the BURST PHASE control, i.e. either locally (at the color phase module front panel) or remotely, make the following modifications in the color phase module circuitry:

a. At the junction of resistors R7 and R8, unsolder the wire which runs to pin 11 of plug P1. Solder the wire to the unused normally open contact of relay K1.

b. At the junction of resistors R7 and R8, unsolder the wire which runs to the center-arm of the SYSTEM PHASE control (potentiometer R2). Solder the wire to the unused normally closed contact of relay K1.

c. Solder a wire between the junction of resistors R7 and R8 and the unused common contact of relay K1. (See figure 75.)

6. To utilize the LOCAL/REMOTE pushbutton switch on the RECORD control panel, proceed as follows:

a. Open the panel so that the pushbutton switch wiring is exposed, and cut the jumper between the normally open and normally closed contacts of section A (4S1A).

b. Solder a long wire to the normally open contact of section A of the pushbutton switch, run the wire with the existing cabling to the receptacle of module no. 232, solder to a spare taper pin, and insert the pin in position 6.

> NOTE: It may be desirable to utilize a separately mounted switch, rather than the LOCAL/REMOTE switch in delegating control of the burst phase (and system phase if the procedure in step 5 has been followed) to a remote location. In this case, all that is necessary is that the switch provide a ground potential to pin 6 of module no. 232 receptacle when it is in "remote" mode.

7. Mount two 10K ohm *Bournes* potentiometers (RCA drawing no. 8546679-105; stock no. 230513) in the remote location. Label one potentiometer SYSTEM PHASE and the other potentiometer BURST PHASE.

8. Make up a remote control cable containing four wires. Solder the wires to pins 1, 2, 3 and 4 of an eight pin plug (RCA stock no. 229751) that mates with the SIGNAL REMOTE connector J26. Connect the plug to J26 at the machine.

9. At the remote location, solder a jumper between the terminal closest to the shaft of the SYSTEM PHASE potentiometer and the terminal closest to the shaft of the BURST PHASE potentiometer, and solder the wire from pin 1 of the remote control cable plug to the jumper.

10. Solder a jumper between the center terminal of the SYSTEM PHASE potentiometer and the center terminal of the BURST PHASE potentiometer, and solder the wire from pin 4 of the remote control cable plug to the jumper.

11. Solder the wire from pin 2 of the remote control cable plug to the center-arm (slider) of the BURST PHASE control.

12. Solder the wire from pin 3 of the remote control cable plug to the center-arm (slider) of the SYSTEM PHASE control.

INSTALLATION IN TR-3/TR-4 MACHINES

Color ATC System

The following procedure is recommended for the installation of the ES-43582 color ATC system in TR-3/TR-4 Television Tape machines. Items referred to in the installation procedure pertain to items contained in MI-43353 and MI-43392, and are described in table III.

1. Remove the blank front panels covering module apertures C11 through C16 in the following manner:

a. Remove modules C17 and C18.

b. Loosen the nuts at the back of the blank panel covering the aperture for modules C15 and C16 with a 5/16-inch open end wrench until the clamps held by the nuts can be rotated 180 degrees.

c. Lift the blank panel up and pull out.

d. Follow the procedures in steps b and c above to remove the blank panel covering the aperture for modules C11 through C14.

e. Re-insert modules C17 and C18 into their proper receptacles.

2. Check the d-c voltage inputs to each color ATC module by inserting a module extender into the module receptacle and measuring the voltages at pins 7, 9, 22, and 25. The voltages measured should be as follows:

Pin 7	−20V
Pin 9	−10V
Pin 22	+70V
Pin 25	−26V

3. Insert the color ATC system modules (items 1 through 6 of MI-43353) into their proper receptacles.

4. Open the hinged control panel and insert the color fixed delay module (item 1 of MI-43392) into its proper receptacle.

5. Check to ascertain that resistor R4 in the sync logic module circuitry is an 820 ohm, ½ watt, 5% resistor. If it is not, replace it at this time.

Remote SYSTEM PHASE and BURST PHASE Controls

Provision is made for remote as well as local control of the system subcarrier and burst subcarrier phasing in the color ATC system. Two procedures for installing the controls are presented below. The first procedure outlines a method of installing the controls in the MI-40692 video remote control panel. (This procedure assumes that the video remote control panel has been installed correctly and its other functions are operating properly.) The second procedure outlines a method of installing the controls in a separate remote control panel.

Installation in the MI-40692 Video Remote Control Panel

1. In the color phase module (no. C16) circuitry remove the jumper which connects the center-arm of the SYSTEM PHASE control (potentiometer R2) to the junction of resistors R7 and R8.

> NOTE: When the jumper has been removed, the SYSTEM PHASE control may be operated only from the remote location (regardless of the mode of the LOCAL/REMOTE switch on the control panel) unless step 2 below is carried out.

2. If it is desired to operate the SYSTEM PHASE control similarly to the BURST PHASE control, i.e. either locally (at the color phase module front panel) or remotely, make the following modifications in the color phase module circuitry:

a. At the junction of resistors R7 and R8, unsolder the wire which runs to pin 11 of plug P1. Solder the wire to the unused normally open contact of relay K1.

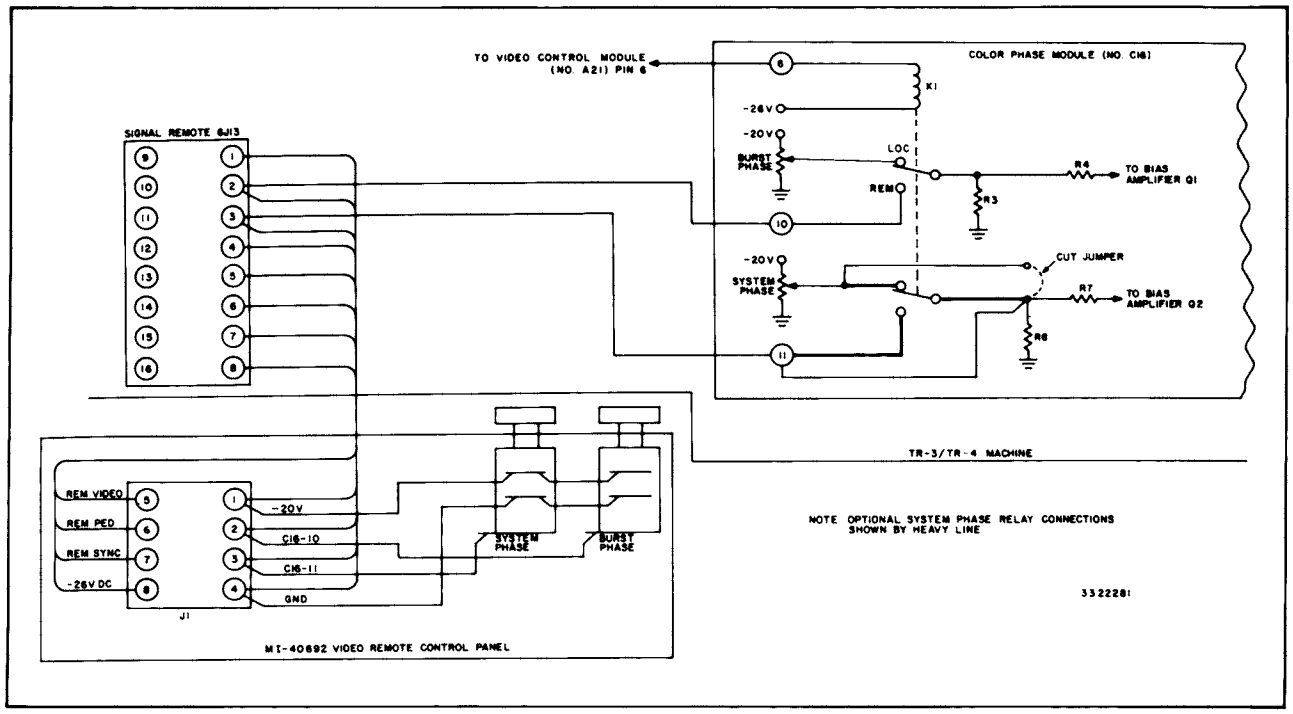


Figure 76—Installation of Burst and System Phase Controls in MI-40692 Video Remote Control Panel (TR-3/TR-4 Machines)

b. At the junction of resistors R7 and R8, unsolder the wire which runs to the center-arm of the SYSTEM PHASE control (potentiometer R2). Solder the wire to the unused normally closed contact of relay K1.

c. Solder a wire between the junction of resistors R7 and R8 and the unused common contact of relay K1. (See figure 76.)

3. Mount two 10K ohm *Bournes* potentiometers (RCA drawing no. 8546679-105; stock no. 230513) on the MI-40692 video remote control panel. Label one potentiometer SYSTEM PHASE and the other potentiometer BURST PHASE.

4. Unsolder the wire connected to pin 3 of jack J1 on the video remote control panel and solder it to pin 4, so that there are now two wires soldered to pin 4.

5. Solder a jumper between the terminal closest to the shaft of the SYSTEM PHASE potentiometer and the terminal closest to the shaft of the BURST PHASE potentiometer, and solder a wire from this jumper to the −20 volt bus of the remote control panel. (−20 volts dc is fed to the remote control panel at pin 1 of jack J1.)

6. Solder a jumper between the center terminal of the SYSTEM PHASE potentiometer and the center terminal of the BURST PHASE potentiometer, and solder a wire from this jumper to the ground bus of the remote control panel. (Ground potential is applied to the remote control panel at pin 4 of jack J1.)

7. Solder a wire between the center-arm (slider) of the SYSTEM PHASE potentiometer and pin 3 of jack J1.

8. Solder a wire between the center-arm (slider) of the BURST PHASE potentiometer and pin 2 of jack J1.

9. Add wires to the existing remote control cable which will connect pin 2 of the SIGNAL REMOTE connector 6J13 (at the machine) to pin 2 of jack J1 (at the remote control panel) and pin 3 of 6J13 to pin 3 of J1.

Installation in a Separate Remote Control Panel

1. In the color phase module (no. C16) circuitry, remove the jumper which connects the center-arm of the SYSTEM PHASE control (potentiometer R2) to the junction of resistors R7 and R8.

> NOTE: When the jumper has been removed, the SYSTEM PHASE control may be operated only from the remote location (regardless of the mode of the LOCAL/REMOTE switch on the control panel) unless step 2 below is carried out.

2. If it is desired to operate the SYSTEM PHASE control similarly to the BURST PHASE control, i.e.

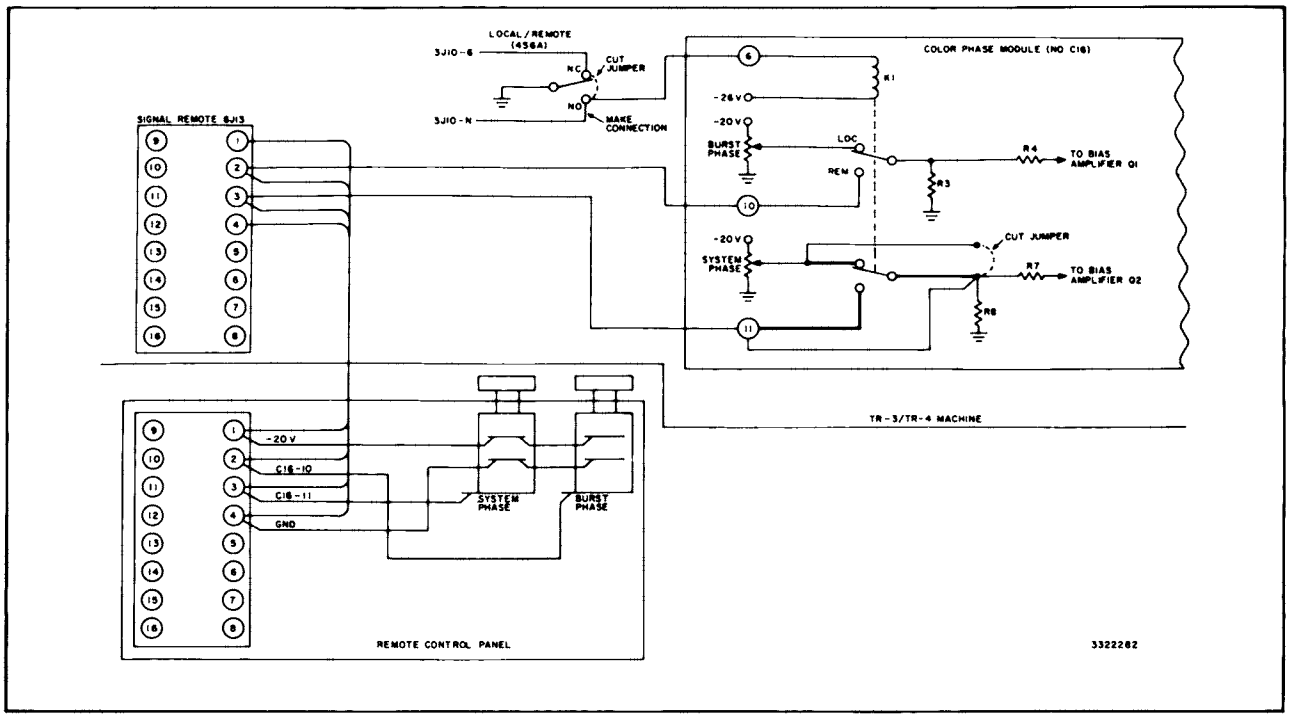


Figure 77—Installation of Burst and System Phase Controls in Separate Remote Control Panel (TR-3/TR-4 Machines)

either locally (at the color phase module front panel) or remotely, make the following modifications in the color phase module circuitry:

a. At the junction of resistors R7 and R8, unsolder the wire which runs to pin 11 of plug P1. Solder the wire to the unused normally open contact of relay K1.

b. At the junction of resistors R7 and R8, unsolder the wire which runs to the center-arm of the SYSTEM PHASE control (potentiometer R2). Solder the wire to the unused normally closed contact of relay K1.

c. Solder a wire between the junction of resistors R7 and R8 and the unused common contact of relay K1. (See figure 77.)

3. To utilize the LOCAL/REMOTE pushbutton switch on the control panel, open the control panel so that the pushbutton switch wiring is exposed and connect the wire from pin N of jack 3J10 (designated 6SA NO) to the normally open (NO) contact of section A of the switch (4S6A).

NOTE: It may be desirable to utilize a separately mounted switch, rather than the LOCAL/REMOTE switch, in delegating control of the burst phase (and system phase if the procedure in step 2 has been followed) to a remote location. In this case, all that is necessary is that the switch provide a ground potential to pin 6 of module no. C16 receptacle when it is in "remote" mode.

4. Mount two 10K ohm *Bournes* potentiometers (RCA drawing no. 8546679-105; stock no. 230513) in the remote location. Label one potentiometer SYSTEM PHASE and the other potentiometer BURST PHASE.

5. Make up a remote control cable containing four wires. Solder the wires to pins 1, 2, 3, and 4 of a sixteen pin plug (RCA stock no. 224605) that mates with the SIGNAL REMOTE connector 6J13. Connect the plug to 6J13 at the machine.

6. At the remote location, solder a jumper to the terminal closest to the shaft of the SYSTEM PHASE potentiometer and the terminal closest to the shaft of the BURST PHASE potentiometer, and solder the wire from pin 1 of the remote control cable plug to the jumper.

7. Solder a jumper between the center terminal of the SYSTEM PHASE potentiometer and the center terminal of the BURST PHASE potentiometer, and solder the wire from pin 4 of the remote control cable plug to the jumper.

8. Solder the wire from pin 2 of the remote control cable plug to the center-arm (slider) of the BURST PHASE control.

9. Solder the wire from pin 3 of the remote control cable plug to the center-arm (slider) of the SYSTEM PHASE control.

LIST OF PARTS

Symbol	Stock No.	Drawing No.	Description
		-	
		-	
		-	
		-	**MI-43353 COLOR ATC MODULES FOR TR-3, TR-4, TR-22**
		-	
		-	
		-	
		8543734-501	**COLOR PROCESSOR MODULE (231/C15)**
		-	
C1	214738	8959154-194	ELECTROLYTIC, 20 MF 100 V
C2	108020	8959154-114	ELECTROLYTIC, 100 MF 25 V
C3	108020	8959154-114	ELECTROLYTIC, 100 MF 25 V
C4	223693	8959154-152	ELECTROLYTIC, 300 MF 3 V
C5	300463	8524007- 47	TANTALUM, 22 MF ±20% 15 V
C6	223693	8959154-152	ELECTROLYTIC, 300 MF 3 V
C7	300463	8524007- 47	TANTALUM, 22 MF ±20% 15 V
C8	217350	8959154-108	ELECTROLYTIC, 10 MF 25 V
C9	219040	8959154-181	ELECTROLYTIC, 100 MF 12 V
C10	108020	8959154-114	ELECTROLYTIC, 100 MF 25 V
C12	223672	990786-175	PLASTIC, 0.1 MF ±10% 100 V
C13	225613	993025-437	MICA, 100 MMF ±5% 100 V
C14	219040	8959154-181	ELECTROLYTIC, 100 MF 12 V
C15	223672	990786-175	PLASTIC, 0.1 MF ±10% 100 V
C16	219040	8959154-181	ELECTROLYTIC, 100 MF 12 V
C17	219040	8959154-181	ELECTROLYTIC, 100 MF 12 V
C18	223672	990786-175	PLASTIC, 0.1 MF ±10% 100 V
C19	219040	8959154-181	ELECTROLYTIC, 100 MF 12 V
C20	223672	990786-175	PLASTIC, 0.1 MF ±10% 100 V
C21	217350	8959154-108	ELECTROLYTIC, 10 MF 25 V
C22	106552	8959154-184	ELECTROLYTIC, 250 MF 12 V
C23	226980	990786-163	PLASTIC, .01 MF ±10% 100 V
C24	226980	990786-163	PLASTIC, .01 MF ±10% 100 V
C25	226980	990786-163	PLASTIC, .01 MF ±10% 100 V
C26	228267	990786-172	PLASTIC, .056 MF ±10% 100 V
C27	226980	990786-163	PLASTIC, .01 MF ±10% 100 V
C28	106940	993025-444	MICA, 200 MMF ±5% 100 V
C29	226980	990786-163	PLASTIC, .01 MF ±10% 100 V
C30	226980	990786-163	PLASTIC, .01 MF ±10% 100 V
C31	226980	990786-163	PLASTIC, .01 MF ±10% 100 V
C32	223672	990786-175	PLASTIC, 0.1 MF ±10% 100 V
C33	108020	8959154-114	ELECTROLYTIC, 100 MF 25 V
C34	219040	8959154-181	ELECTROLYTIC, 100 MF 12 V
C35	219039	8959154-110	ELECTROLYTIC, 25 MF 25 V
C36	225608	993025-424	MICA, 30 MMF ±5% 100 V
C37	225608	993025-424	MICA, 30 MMF ±5% 100 V
C38	225619	993025-466	MICA, 1600 MMF ±5% 100 V
C39	217350	8959154-108	ELECTROLYTIC, 10 MF 25 V
C40	217350	8959154-108	ELECTROLYTIC, 10 MF 25 V
C41	217350	8959154-108	ELECTROLYTIC, 10 MF 25 V
C42	217350	8959154-108	ELECTROLYTIC, 10 MF 25 V
C43	260053	993025-460	MICA, 910 MMF ±5% 100 V
C44	219195	993025-461	MICA, 1000 MMF ±5% 100 V
C45	300198	993025-457	MICA, 680 MMF ±5% 100 V
C46	223672	990786-175	PLASTIC, 0.1 MF ±10% 100 V
C47	106552	8959154-184	ELECTROLYTIC, 250 MF 12 V
C48	106552	8959154-184	ELECTROLYTIC, 250 MF 12 V
C49	224417	8524008-401	TANTALUM, 100 MF ±10% 20 V
		-	
CR1 TO		-	
CR10	225584	-	DIODE - TYPE 1N100A
CR11	225592	-	DIODE - TYPE 1N3253
CR12	225592	-	DIODE - TYPE 1N3253
CR13	225584	-	DIODE - TYPE 1N100A
CR14	225584	-	DIODE - TYPE 1N100A
CR15	225592	-	DIODE - TYPE 1N3253
CR16	225592	-	DIODE - TYPE 1N3253
CR17	225592	-	DIODE - TYPE 1N3253
CR18	225592	-	DIODE - TYPE 1N3253
K1	255800	8526088- 2	RELAY
K2	255800	8526088- 2	RELAY
L1	205878	8825473-505	COIL - 10 MILLIHENRY
P1	230443	8526621- 42	CONNECTOR

Symbol	Stock No.	Drawing No.	Description
Q1	223685	-	TRANSISTOR - TYPE 2N1309
Q2	226685	-	TRANSISTOR - TYPE 2N2270
Q3	223685	-	TRANSISTOR - TYPE 2N1309
Q4	224548	-	TRANSISTOR - TYPE 2N1169
Q5	224548	-	TRANSISTOR - TYPE 2N1169
Q6	226441	-	TRANSISTOR - TYPE 2N1306
Q7	226442	-	TRANSISTOR - TYPE 2N1307
Q8	226442	-	TRANSISTOR - TYPE 2N1307
Q9	223685	-	TRANSISTOR - TYPE 2N1309
Q10	226685	-	TRANSISTOR - TYPE 2N2270
Q11	223684	-	TRANSISTOR - TYPE 2N1308
Q12	223685	-	TRANSISTOR - TYPE 2N1309
Q13	223684	-	TRANSISTOR - TYPE 2N1308
Q14	223685	-	TRANSISTOR - TYPE 2N1309
Q15	226441	-	TRANSISTOR - TYPE 2N1306
Q16	226441	-	TRANSISTOR - TYPE 2N1306
Q17	226442	-	TRANSISTOR - TYPE 2N1307
Q18	226442	-	TRANSISTOR - TYPE 2N1307
Q21	229133	-	TRANSISTOR - TYPE 2N2189
Q22	226685	-	TRANSISTOR - TYPE 2N2270
Q23	229133	-	TRANSISTOR - TYPE 2N2189
Q24	221856	-	TRANSISTOR - TYPE 2N1301
Q25	221856	-	TRANSISTOR - TYPE 2N1301
Q26	221856	-	TRANSISTOR - TYPE 2N1301
Q27	226239	-	TRANSISTOR - TYPE 2N706A
Q28	226239	-	TRANSISTOR - TYPE 2N706A
Q29	226239	-	TRANSISTOR - TYPE 2N706A
Q30	226239	-	TRANSISTOR - TYPE 2N706A
Q31	229133	-	TRANSISTOR - TYPE 2N2189
Q32	226239	-	TRANSISTOR - TYPE 2N706A
Q33	226239	-	TRANSISTOR - TYPE 2N706A
Q34	226238	-	TRANSISTOR - TYPE 2N1319
Q35	226441	-	TRANSISTOR - TYPE 2N1306
		-	
R1	236069	990476-329	FILM, 1960 OHMS ±1% 1/2 W
R2	236097	990476-458	FILM, 39,200 OHMS ±1% 1/2 W
R3	502322	82283-191	22,000 OHMS ±5% 1/2 W
R4	502110	82283-135	100 OHMS ±5% 1/2 W
R5	502316	82283-188	16,000 OHMS ±5% 1/2 W
R6	502324	82283-192	24,000 OHMS ±5% 1/2 W
R7	229881	8980004-126	VARIABLE, 500 OHMS 1 W
R8	502168	82283-155	680 OHMS ±5% 1/2 W
R9	502275	82283-180	7500 OHMS ±5% 1/2 W
R10	502130	82283-146	300 OHMS ±5% 1/2 W
R11	236054	990476-249	FILM, 316 OHMS ±1% 1/2 W
R12	236088	990476-405	FILM, 11,000 OHMS ±1% 1/2 W
R13	236095	990476-441	FILM, 26,100 OHMS ±1% 1/2 W
R14	236092	990476-425	FILM, 17,800 OHMS ±1% 1/2 W
R15	236094	990476-437	FILM, 23,700 OHMS ±1% 1/2 W
R16	236084	990476-385	FILM, 7500 OHMS ±1% 1/2 W
R17	236078	990476-357	FILM, 3830 OHMS ±1% 1/2 W
R18	236089	990476-409	FILM, 12,100 OHMS ±1% 1/2 W
R19	236085	990476-389	FILM, 8250 OHMS ±1% 1/2 W
R20	236086	990476-393	FILM, 9090 OHMS ±1% 1/2 W
R21	236083	990476-377	FILM, 6190 OHMS ±1% 1/2 W
R22	236050	990476-181	FILM, 68,100 OHMS ±1% 1/2 W
R23	236050	990476-181	FILM, 68,100 OHMS ±1% 1/2 W
R24	236049	990476-169	FILM, 51,100 OHMS ±1% 1/2 W
R25	236049	990476-169	FILM, 51,100 OHMS ±1% 1/2 W
R26	236049	990476-169	FILM, 51,100 OHMS ±1% 1/2 W
R27	236048	990476-153	FILM, 34,800 OHMS ±1% 1/2 W
R28	236046	990476-129	FILM, 19,600 OHMS ±1% 1/2 W
R29	236045	990476-125	FILM, 17,800 OHMS ±1% 1/2 W
R30	236047	990476-133	FILM, 21,500 OHMS ±1% 1/2 W
R31	236048	990476-153	FILM, 34,800 OHMS ±1% 1/2 W
R32	502015	82283-115	15 OHMS ±5% 1/2 W
R33	235621	990476-347	FILM, 3010 OHMS ±1% 1/2 W
R34	236075	990476-345	FILM, 2870 OHMS ±1% 1/2 W
R35	235621	990476-347	FILM, 3010 OHMS ±1% 1/2 W
R36	229880	8980004-125	VARIABLE, 200 OHMS 1 W
R37	502268	82283-179	6800 OHMS ±5% 1/2 W
R38	236107	990477-230	FILM, 200 OHMS ±1% 1 W

Symbol	Stock No.	Drawing No.	Description
R39	512118	90496-141	180 OHMS ±5% 1 W
R40	229879	8980004-123	VARIABLE, 50 OHMS 1 W
R41	502039	82283-125	39 OHMS ±5% 1/2 W
R42	502233	82283-171	3300 OHMS ±5% 1/2 W
R43	502216	82283-164	1600 OHMS ±5% 1/2 W
R44	229879	8980004-123	VARIABLE, 50 OHMS 1 W
R45	502010	82283-111	10 OHMS ±5% 1/2 W
R46	502315	82283-187	15,000 OHMS ±5% 1/2 W
R47	502233	82283-171	3300 OHMS ±5% 1/2 W
R48	229879	8980004-123	VARIABLE, 50 OHMS 1 W
R49	502010	82283-111	10 OHMS ±5% 1/2 W
R50	502111	82283-136	110 OHMS ±5% 1/2 W
R51	502210	82283-159	1000 OHMS ±5% 1/2 W
R52	502111	82283-136	110 OHMS ±5% 1/2 W
R53	236072	990476-337	FILM, 2370 OHMS ±1% 1/2 W
R54	502210	82283-159	1000 OHMS ±5% 1/2 W
R55	502336	82283-196	36,000 OHMS ±5% 1/2 W
R56	236100	990476-469	FILM, 51,100 OHMS ±1% 1/2 W
R57	236066	990476-317	FILM, 1470 OHMS ±1% 1/2 W
R58	236075	990476-345	FILM, 2870 OHMS ±1% 1/2 W
R59	236080	990476-365	FILM, 4640 OHMS ±1% 1/2 W
R60	236065	990476-313	FILM, 1330 OHMS ±1% 1/2 W
R61	502347	82283-199	47,000 OHMS ±5% 1/2 W
R62	236100	990476-469	FILM, 51,100 OHMS ±1% 1/2 W
R63	236066	990476-317	FILM, 1470 OHMS ±1% 1/2 W
R64	229880	8980004-125	VARIABLE, 200 OHMS 1 W
R65	236058	990476-281	FILM, 681 OHMS ±1% 1/2 W
R66	502151	82283-152	510 OHMS ±5% 1/2 W
R67	502224	82283-168	2400 OHMS ±5% 1/2 W
R68	502210	82283-159	1000 OHMS ±5% 1/2 W
R69	502010	82283-111	10 OHMS ±5% 1/2 W
R70	502368	82283-203	68,000 OHMS ±5% 1/2 W
R71	502336	82283-172	3600 OHMS ±5% 1/2 W
R72	502215	82283-163	1500 OHMS ±5% 1/2 W
R73	502010	82283-111	10 OHMS)5% 1/2 W
R74	502233	82283-171	3300 OHMS ±5% 1/2 W
R75	502320	82283-190	20,000 OHMS ±5% 1/2 W
R76	502222	82283-167	2200 OHMS ±5% 1/2 W
R77	236087	990476-401	FILM, 10,000 OHMS ±1% 1/2 W
R78	236087	990476-401	FILM, 10,000 OHMS ±1% 1/2 W
R81	236091	990476-417	FILM, 14,700 OHMS ±1% 1/2 W
R82	502075	82283-132	75 OHMS ±5% 1/2 W
R83	236064	990476-309	FILM, 1210 OHMS ±1% 1/2 W
R84	502110	82283-135	100 OHMS ±5% 1/2 W
R85	502139	82283-149	390 OHMS ±5% 1/2 W
R86	502222	82283-167	2200 OHMS ±5% 1/2 W
R87	502020	82283-118	20 OHMS ±5% 1/2 W
R88	502139	82283-149	390 OHMS ±5% 1/2 W
R89	502222	82283-167	2200 OHMS ±5% 1/2 W
R90	502210	82283-159	1000 OHMS ±5% 1/2 W
R91	502210	82283-159	1000 OHMS ±5% 1/2 W
R92	502130	82283-146	300 OHMS ±5% 1/2 W
R93	229881	8980004-126	VARIABLE, 500 OHMS 1 W
R94	502210	82283-159	1000 OHMS ±5% 1/2 W
R95	226676	8971860-905	VARIABLE, 500 OHMS 2 W
R96	502127	82283-145	270 OHMS ±5% 1/2 W
R97	502010	82283-111	10 OHMS ±5% 1/2 W
R98	502168	82283-155	680 OHMS ±5% 1/2 W
R99	502247	82283-175	4700 OHMS ±5% 1/2 W
R100	502247	82283-175	4700 OHMS ±5% 1/2 W
R101	502120	82283-142	200 OHMS ±5% 1/2 W
R102	502310	82283-183	10,000 OHMS ±5% 1/2 W
R103	502151	82283-152	510 OHMS ±5% 1/2 W
R104	502151	82283-152	510 OHMS ±5% 1/2 W
R105	502143	82283-150	430 OHMS ±5% 1/2 W
R106	502010	82283-111	10 OHMS ±5% 1/2 W
R107	502310	82283-183	10,000 OHMS ±5% 1/2 W
R108	502310	82283-183	10,000 OHMS ±5% 1/2 W
R109	502139	82283-149	390 OHMS ±5% 1/2 W
R110	502020	82283-118	20 OHMS ±5% 1/2 W
R111	502210	82283-159	1000 OHMS ±5% 1/2 W
R112	502111	82283-136	110 OHMS ±5% 1/2 W

Symbol	*Stock No.*	*Drawing No.*	*Description*
R113	502133	82283-147	330 OHMS ±5% 1/2 W
R114	502322	82283-191	22,000 OHMS ±5% 1/2 W
R115	502247	82283-175	4700 OHMS ±5% 1/2 W
R116	502075	82283-132	75 OHMS ±5% 1/2 W
R117	502210	82283-159	1000 OHMS ±5% 1/2 W
R118	502230	82283-170	3000 OHMS ±5% 1/2 W
R119	502310	82283-183	10,000 OHMS ±5% 1/2 W
R120	502233	82283-171	3300 OHMS ±5% 1/2 W
R121	502191	82283-158	910 OHMS ±5% 1/2 W
R122	502291	82283-182	9100 OHMS ±5% 1/2 W
R123	502182	82283-157	820 OHMS ±5% 1/2 W
R124	502191	82283-158	910 OHMS ±5% 1/2 W
R125	502291	82283-182	9100 OHMS ±5% 1/2 W
R126	502182	82283-157	820 OHMS ±5% 1/2 W
R127	502315	82283-187	15,000 OHMS ±5% 1/2 W
R128	502210	82283-159	1000 OHMS ±5% 1/2 W
R129	502215	82283-163	1500 OHMS ±5% 1/2 W
R130	502182	82283-157	820 OHMS ±5% 1/2 W
R131	502220	82283-166	2000 OHMS ±5% 1/2 W
R132	236060	990476-289	FILM, 825 OHMS ±1% 1/2 W
R133	236060	990476-289	FILM, 825 OHMS ±1% 1/2 W
R134	502151	82283-152	510 OHMS ±5% 1/2 W
R135	502215	82283-163	1500 OHMS ±5% 1/2 W
R136	502415	82283-211	150,000 OHMS ±5% 1/2 W
R137	502222	82283-167	2200 OHMS ±5% 1/2 W
R138	232479	8980004-129	VARIABLE, 5000 OHMS 1 W
R139	502247	82283-175	4700 OHMS ±5% 1/2 W
R140	502247	82283-175	4700 OHMS ±5% 1/2 W
R141	230489	8980004-132	VARIABLE, 25,000 OHMS 1 W
R142	502427	82283-217	270,000 OHMS ±5% 1/2 W
R143	502310	82283-183	10,000 OHMS ±5% 1/2 W
R144	502312	82283-185	12,000 OHMS ±5% 1/2 W
R145	502239	82283-173	3900 OHMS ±5% 1/2 W
R146	502020	82283-118	20 OHMS ±5% 1/2 W
R147	502010	82283-111	10 OHMS ±5% 1/2 W
R148	502220	82283-166	2000 OHMS ±5% 1/2 W
R149	502210	82283-159	1000 OHMS ±5% 1/2 W
R150	502162	82283-154	620 OHMS ±5% 1/2 W
R151	502182	82283-157	820 OHMS ±5% 1/2 W
R152	502251	82283-176	5100 OHMS ±5% 1/2 W
R153	232479	8980004-129	VARIABLE, 5000 OHMS 1 W
R154	502313	82283-186	13,000 OHMS ±5% 1/2 W
R155	502230	82283-170	3000 OHMS ±5% 1/2 W
R156	230487	8980004-127	VARIABLE, 1000 OHMS 1 W
R157	234462	8527503- 3	WIREWOUND, 2 OHMS ±5% 2 W
R158	502330	82283-194	30,000 OHMS ±5% 1/2 W
R159	502330	82283-194	30,000 OHMS ±5% 1/2 W
		-	
S1	225773	8526094- 2	SWITCH - BLACK
TP1	214603	8941099- 4	JACK - TIP, YELLOW
TP2	214603	8941099- 4	JACK - TIP, YELLOW
TP3	214603	8941099- 4	JACK - TIP, YELLOW
Z1	229087	-	DIODE - TYPE 1N4243
Z2	229087	-	DIODE - TYPE 1N4243
Z3	229087	-	DIODE - TYPE 1N4243
Z4	230463	-	DIODE - TYPE 1N4242
		-	
		-	
		8543735-501	**COLOR PHASE MODULE (232/C16)**
		-	
C1	217350	8959154-108	ELECTROLYTIC, 10 MF 25 V
C2	217350	8959154-108	ELECTROLYTIC, 10 MF 25 V
C3	223672	990786-175	PLASTIC, 0.1 MF ±10% 100 V
C4	300753	990786-165	PLASTIC, .015 MF ±10% 100 V
C5	223672	990786-175	PLASTIC, 0.1 MF ±10% 100 V
C6	300753	990786-165	PLASTIC, .015 MF ±10% 100 V
C7	300753	990786-165	PLASTIC, .015 MF ±10% 100 V
C8	214738	8959154-194	ELECTROLYTIC, 20 MF 100 V
C9	300753	990786-165	PLASTIC, .015 MF ±10% 100 V
C10	224417	8524008-601	TANTALUM, 100 MF ±20% 20 V
C11	223672	990786-175	PLASTIC, 0.1 MF ±10% 50 V
C12	224417	8524008-601	TANTALUM, 100 MF ±20% 20 V

Symbol	Stock No.	Drawing No.	Description
C13	223672	990786-175	PLASTIC, 0.1 MF ±10% 100 V
C14	223672	990786-175	PLASTIC, 0.1 MF ±10% 100 V
C15	300753	990786-165	PLASTIC, .015 MF ±10% 100 V
C16	300753	990786-165	PLASTIC, .015 MF ±10% 100 V
C17	300753	990786-165	PLASTIC, .015 MF ±10% 100 V
C18	300753	990786-165	PLASTIC, .015 MF ±10% 100 V
		-	
CR1	225592	-	DIODE - TYPE 2N3253
CR2	225584	-	DIODE - TYPE 1N100A
CR3	225584	-	DIODE - TYPE 1N100A
CR4	230511	8528891- 4	DIODE
CR5	230511	8528891- 4	DIODE
CR6 TO		-	
CR23	223687	8528891- 1	DIODE
CR24	230511	8528891- 4	DIODE
CR25	230511	8528891- 4	DIODE
CR26	230511	8528891- 4	DIODE
CR27	230511	8528891- 4	DIODE
CR28		-	
TO		-	
CR45	223687	8528891- 1	DIODE
CR46	230511	8528891- 4	DIODE
CR47	230511	8528891- 4	DIODE
CR48	225592	-	DIODE - TYPE 2N3253
CR49	225592	-	DIODE - TYPE 2N3253
CR50	225592	-	DIODE - TYPE 2N3253
DL1	236204	8497121-501	DELAY LINE ASSEMBLY
DL2	236204	8497121-501	DELAY LINE ASSEMBLY
K1	255800	8526088- 2	RELAY - 975 OHMS
L1	204681	8825473-508	COIL - 25 MICROHENRY
L2	99792	8825473-506	COIL - 15 MICROHENRY
L3	99792	8825473-506	COIL - 15 MICROHENRY
L4	99792	8825473-506	COIL - 15 MICROHENRY
L25	205518	8825473-507	COIL - 20 MICROHENRY
P1	230444	8526621- 43	CONNECTOR - 32 PIN
Q1	226685	-	TRANSISTOR - TYPE 2N2270
Q2	226685	-	TRANSISTOR - TYPE 2N2270
Q3	258993	-	TRANSISTOR - TYPE 2N1304
Q4	226442	-	TRANSISTOR - TYPE 2N1307
Q5	225598	-	TRANSISTOR - TYPE 2N1183
Q6 TO		-	
Q12	229133	-	TRANSISTOR - TYPE 2N2189
		-	
R1	230513	8546679-105	VARIABLE, 10,000 2 W
R2	230513	8546679-105	VARIABLE, 10,000 2 W
R3	236068	990476-325	FILM, 1780 OHMS ±1% 1/2 W
R4	502110	82283-135	100 OHMS ±5% 1/2 W
R5	236083	990476-377	FILM, 6190 OHMS ±1% 1/2 W
R6	236058	990476-281	FILM, 681 OHMS ±1% 1/2 W
R7	236068	990476-325	FILM, 1780 OHMS ±1% 1/2 W
R8	502110	82283-135	100 OHMS ±5% 1/2 W
R9	236083	990476-377	FILM, 6190 OHMS ±1% 1/2 W
R10	236058	990476-281	FILM, 681 OHMS ±1% 1/2 W
R11	236094	990476-437	FILM, 23,700 OHMS ±1% 1/2 W
R12	236087	990476-401	FILM, 10,000 OHMS ±1% 1/2 W
R13	502251	82283-176	5100 OHMS ±5% 1/2 W
R14	236087	990476-401	FILM, 10,000 OHMS ±1% 1/2 W
R15	236094	990476-437	FILM, 23,700 OHMS ±1% 1/2 W
R16	236087	990476-401	FILM, 10,000 OHMS ±1% 1/2 W
R17	502251	82283-176	5100 OHMS ±5% 1/2 W
R18	236087	990476-401	FILM, 10,000 OHMS ±1% 1/2 W
R19	502110	82283-135	100 OHMS ±5% 1/2 W
R20	502315	82283-187	15,000 OHMS ±5% 1/2 W
R21	502312	82283-185	12,000 OHMS ±5% 1/2 W
R22	502210	82283-159	1000 OHMS ±5% 1/2 W
R23	502233	82283-195	3300 OHMS ±5% 1/2 W
R24	502368	82283-203	68,000 OHMS ±5% 1/2 W
R25	502312	82283-185	12,000 OHMS ±5% 1/2 W
R26	502415	82283-211	150,000 OHMS ±5% 1/2 W
R27	502120	82283-142	200 OHMS ±5% 1/2 W
R28	229881	8980004-126	VARIABLE, 500 OHMS 1 W
R29	502139	82283-149	390 OHMS ±5% 1/2 W

Symbol	Stock No.	Drawing No.	Description
R30	502320	82283-190	20,000 OHMS ±5% 1/2 W
R31	502215	82283-163	1500 OHMS ±5% 1/2 W
R32	502212	82283-161	1200 OHMS ±5% 1/2 W
R33	502068	82283-131	68 OHMS ±5% 1/2 W
R34	502168	82283-155	680 OHMS ±5% 1/2 W
R35	502022	82283-119	22 OHMS ±5% 1/2 W
R36	502022	82283-119	22 OHMS ±5% 1/2 W
R37	502220	82283-166	2000 OHMS ±5% 1/2 W
R38	502112	82283-137	120 OHMS ±5% 1/2 W
R39	502212	82283-161	1200 OHMS ±5% 1/2 W
R40	229881	8980004-126	VARIABLE, 500 OHMS 1 W
R41	502139	82283-149	390 OHMS ±5% 1/2 W
R42	502320	82283-190	20,000 OHMS ±5% 1/2 W
R43	502211	82283-160	1100 OHMS ±5% 1/2 W
R44	502068	82283-131	68 OHMS ±5% 1/2 W
R45	502275	82283-180	7500 OHMS ±5% 1/2 W
R46	502222	82283-167	2200 OHMS ±5% 1/2 W
R47	502222	82283-167	2200 OHMS ±5% 1/2 W
R48	502139	82283-149	390 OHMS ±5% 1/2 W
R49	502310	82283-183	10,000 OHMS ±5% 1/2 W
R50	502168	82283-155	680 OHMS ±5% 1/2 W
R51	502227	82283-169	2700 OHMS ±5% 1/2 W
R52	502212	82283-161	1200 OHMS ±5% 1/2 W
R53	502191	82283-158	910 OHMS ±5% 1/2 W
		-	
TP1	214603	8941099- 4	JACK - TIP, YELLOW
TP2	214603	8941099- 4	JACK - TIP, YELLOW
TP3	214603	8941099- 4	JACK - TIP, YELLOW
	225743	8527581- 1	KNOB
		-	
		-	
		8543736-501	**COLOR SENSOR MODULE (323/C11)**
		-	
C1	226980	990786-163	PLASTIC, .01 MF ±10% 100 V
C2	219000	993025-438	MICA, 110 MMF ±5% 100 V
C3	108020	8959154-114	ELECTROLYTIC, 100 MF 25 V
C4	226980	990786-163	PLASTIC, .01 MF ±10% 100 V
C6	226980	990786-163	PLASTIC, .01 MF ±10% 100 V
C7	226980	990786-163	PLASTIC, .01 MF ±10% 100 V
C8	221890	8959154-101	ELECTROLYTIC, 1 MF 25 V
C9	224601	993025-464	MICA, 1300 MMF ±5% 100 V
C10	269540	990786-182	PLASTIC, 0.39 MF ±10% 100 V
C11	217350	8959154-108	ELECTROLYTIC, 10 MF 25 V
C12	225662	8528275-480	MICA, 6200 MMF ±5% 100 V
C13	300190	993025-453	MICA, 470 MMF ±5% 100 V
C14	300190	993025-453	MICA, 470 MMF ±5% 100 V
C15	219040	8959154-181	ELECTROLYTIC, 100 MF 12 V
C16	214738	8959154-194	ELECTROLYTIC, 20 MF 100 V
C17	300190	993025-453	MICA, 470 MMF ±5% 100 V
C18	300193	993025-457	MICA, 680 MMF ±5% 100 V
C19	225662	8528275-480	MICA, 6200 MMF ±5% 100 V
C20	300190	993025-453	MICA, 470 MMF ±5% 100 V
C21	218614	8959154-129	ELECTROLYTIC, 100 MF 6 V
C22	218614	8959154-129	ELECTROLYTIC, 100 MF 6 V
C23	226980	990786-163	PLASTIC, .01 MF ±10% 100 V
C24	225662	8528275-480	MICA, 6200 MMF ±5% 100 V
C25	300193	993025-457	MICA, 680 MMF ±5% 100 V
C26	300190	993025-453	MICA, 470 MMF ±5% 100 V
C27	225615	993025-441	MICA, 150 MMF ±5% 100 V
C28	225625	993025-476	MICA, 4300 MMF ±5% 100 V
C29	300190	993025-453	MICA, 470 MMF ±5% 100 V
C30	300190	993025-453	MICA, 470 MMF ±5% 100 V
C31	108020	8959154-114	ELECTROLYTIC, 100 MF 25 V
C32	106552	8959154-184	ELECTROLYTIC, 250 MF 12 V
		-	
CR1	226546	-	DIODE - TYPE 1N3063
CR2	225584	-	DIODE - TYPE 1N100A
CR3	226546	-	DIODE - TYPE 1N3063
CR4	225584	-	DIODE - TYPE 1N100A
CR5	225584	-	DIODE - TYPE 1N100A
CR6	226546	-	DIODE - TYPE 1N3063
CR7	225584	-	DIODE - TYPE 1N100A

Symbol	Stock No.	Drawing No.	Description
CR8	225584	-	DIODE - TYPE 1N100A
CR9	226546	-	DIODE - TYPE 1N3063
CR10	225584	-	DIODE - TYPE 1N100A
CR11	225584	-	DIODE - TYPE 1N100A
CR12	225584	-	DIODE - TYPE 1N100A
CR13	225584	-	DIODE - TYPE 1N100A
L1	230486	8546652- 83	COIL - 7.5-18 MICROHENRY
P1	230445	8526621- 44	CONNECTOR - MALE, 32 PIN
Q1	229133	-	TRANSISTOR - TYPE 2N2189
Q2	226685	-	TRANSISTOR - TYPE 2N2270
Q3	229133	-	TRANSISTOR - TYPE 2N2189
Q4	226685	-	TRANSISTOR - TYPE 2N2270
Q5	226441	-	TRANSISTOR - TYPE 2N1306
Q6	226441	-	TRANSISTOR - TYPE 2N1306
Q7	226442	-	TRANSISTOR - TYPE 2N1307
Q8	223685	-	TRANSISTOR - TYPE 2N1309
Q9	229133	-	TRANSISTOR - TYPE 2N2189
Q10	226685	-	TRANSISTOR - TYPE 2N2270
Q11	226685	-	TRANSISTOR - TYPE 2N2270
Q12	226442	-	TRANSISTOR - TYPE 2N1307
Q13	229133	-	TRANSISTOR - TYPE 2N2189
Q14	226442	-	TRANSISTOR - TYPE 2N1307
Q15	226685	-	TRANSISTOR - TYPE 2N2270
Q16	226685	-	TRANSISTOR - TYPE 2N2270
Q17	226442	-	TRANSISTOR - TYPE 2N1307
Q18	223685	-	TRANSISTOR - TYPE 2N1309
Q19	226441	-	TRANSISTOR - TYPE 2N1306
Q20	229133	-	TRANSISTOR - TYPE 2N2189
Q21	226442	-	TRANSISTOR - TYPE 2N1307
Q22	226685	-	TRANSISTOR - TYPE 2N2270
Q23	226685	-	TRANSISTOR - TYPE 2N2270
Q24	226442	-	TRANSISTOR - TYPE 2N1307
Q25	226442	-	TRANSISTOR - TYPE 2N1307
Q26	226442	-	TRANSISTOR - TYPE 2N1307
		-	
R1	502210	82283-159	1000 OHMS ±5% 1/2 W
R2	502233	82283-171	3300 OHMS ±5% 1/2 W
R3	502215	82283-163	1500 OHMS ±5% 1/2 W
R4	502218	82283-165	1800 OHMS ±5% 1/2 W
R5	502247	82283-175	4700 OHMS ±5% 1/2 W
R6	502022	82283-119	22 OHMS ±5% 1/2 W
R7	502210	82283-159	1000 OHMS ±5% 1/2 W
R8	502118	82283-141	180 OHMS ±5% 1/2 W
R9	229881	8980004-126	VARIABLE, 500 OHMS 1 W
R10	502336	82283-196	36,000 OHMS ±5% 1/2 W
R11	502262	82283-178	6200 OHMS ±5% 1/2 W
R12	502210	82283-159	1000 OHMS ±5% 1/2 W
R13	502216	82283-164	1600 OHMS ±5% 1/2 W
R14	502315	82283-187	15,000 OHMS ±5% 1/2 W
R15	502310	82283-183	10,000 OHMS ±5% 1/2 W
R16	502343	82283-198	43,000 OHMS ±5% 1/2 W
R17	502210	82283-159	1000 OHMS ±5% 1/2 W
R18	502291	82283-182	9100 OHMS ±5% 1/2 W
R19	502210	82283-135	100 OHMS ±5% 1/2 W
R20	502391	82283-206	91,000 OHMS ±5% 1/2 W
R21	502320	82283-190	20,000 OHMS ±5% 1/2 W
R22	502224	82283-168	2400 OHMS ±5% 1/2 W
R23	502210	82283-159	1000 OHMS ±5% 1/2 W
R24	236103	990476-490	FILM, 84,500 OHMS ±1% 1/2 W
R25	236069	990476-329	FILM, 1960 OHMS ±1% 1/2 W
R26	236076	990476-349	FILM, 3160 OHMS ±1% 1/2 W
R27	502220	82283-166	2000 OHMS ±5% 1/2 W
R28	236091	990476-417	FILM, 14,700 OHMS ±1% 1/2 W
R29	502215	82283-163	1500 OHMS ±5% 1/2 W
R30	502230	82283-170	3000 OHMS ±5% 1/2 W
R31	502312	82283-185	12,000 OHMS ±5% 1/2 W
R32	502210	82283-159	1000 OHMS ±5% 1/2 W
R33	502230	82283-170	3000 OHMS ±5% 1/2 W
R34	502375	82283-204	75,000 OHMS ±5% 1/2 W
R35	225732	8527503- 41	WIREWOUND, 470 OHMS ±5% 2 W
R36	502010	82283-111	10 OHMS ±5% 1/2 W
R37	502110	82283-135	100 OHMS ±5% 1/2 W

Symbol	Stock No.	Drawing No.	Description
R40	236063	990476-305	FILM, 1100 OHMS ±1% 1/2 W
R41	236061	990476-293	FILM, 909 OHMS ±1% 1/2 W
R42	502220	82283-166	2000 OHMS ±5% 1/2 W
R43	502156	82283-153	560 OHMS ±5% 1/2 W
R44	229881	8980004-126	VARIABLE, 500 OHMS 1 W
R45	502210	82283-159	1000 OHMS ±5% 1/2 W
R46	236089	990476-409	FILM, 12,100 OHMS ±1% 1/2 W
R47	502215	82283-163	1500 OHMS ±5% 1/2 W
R48	502230	82283-170	3000 OHMS ±5% 1/2 W
R49	502320	82283-190	20,000 OHMS ±5% 1/2 W
R50	502320	82283-190	20,000 OHMS ±5% 1/2 W
R51	502312	82283-185	12,000 OHMS ±5% 1/2 W
R52	502210	82283-159	1000 OHMS ±5% 1/2 W
R53	502230	82283-170	3000 OHMS ±5% 1/2 W
R54	502375	82283-204	75,000 OHMS ±5% 1/2 W
R55	225732	8527503- 41	WIREWOUND, 470 OHMS ±5% 2 W
R56	236065	990476-313	FILM, 1330 OHMS ±1% 1/2 W
R57	236099	990476-465	FILM, 46,400 OHMS ±1% 1/2 W
R58	236070	990476-333	FILM, 2150 OHMS ±1% 1/2 W
R59	236079	990476-361	FILM, 4220 OHMS ±1% 1/2 W
R60	236069	990476-329	FILM, 1960 OHMS ±1% 1/2 W
R61	502412	82283-209	120,000 OHMS ±5% 1/2 W
R62	236101	990476-481	FILM, 68,100 OHMS ±1% 1/2 W
R63	502220	82283-166	2000 OHMS ±5% 1/2 W
R64	236080	990476-365	FILM, 4640 OHMS ±1% 1/2 W
R65	236062	990476-301	FILM, 1000 OHMS ±1% 1/2 W
R66	236091	990476-417	FILM, 14,700 OHMS ±1% 1/2 W
R67	236052	990476-241	FILM, 261 OHMS ±1% 1/2 W
R68	502215	82283-163	1500 OHMS ±5% 1/2 W
R69	502230	82283-170	3000 OHMS ±5% 1/2 W
R70	502415	82283-211	150,000 OHMS ±5% 1/2 W
R71	502320	82283-190	20,000 OHMS ±5% 1/2 W
R72	502324	82283-192	24,000 OHMS ±5% 1/2 W
R73	502312	82283-185	12,000 OHMS ±5% 1/2 W
R74	502210	82283-159	1000 OHMS ±5% 1/2 W
R75	502233	82283-171	3300 OHMS ±5% 1/2 W
R76	502310	82283-183	10,000 OHMS ±5% 1/2 W
R77	502182	82283-157	820 OHMS ±5% 1/2 W
R78	502427	82283-217	270,000 OHMS ±5% 1/2 W
R79	502230	82283-170	3000 OHMS ±5% 1/2 W
R80	502210	82283-159	1000 OHMS ±5% 1/2 W
R81	502224	82283-168	2400 OHMS ±5% 1/2 W
R82	502427	82283-217	270,000 OHMS ±5% 1/2 W
R83	225732	8527503- 41	WIREWOUND, 470 OHMS ±5% 2 W
R84	502320	82283-190	20,000 OHMS ±5% 1/2 W
R85	502320	82283-190	20,000 OHMS ±5% 1/2 W
R86	236099	990476-465	FILM, 46,400 OHMS ±1% 1/2 W
R87	502022	82283-119	22 OHMS ±5% 1/2 W
R88	502010	82283-111	10 OHMS ±5% 1/2 W
		-	
TP1	214603	8941099- 4	JACK - TIP, YELLOW
TP2	214603	8941099- 4	JACK - TIP, YELLOW
TP3	214603	8941099- 4	JACK - TIP, YELLOW
		-	
		-	
		8543737-501	**COLOR DELAY MODULE (324/C12)**
		-	
C1	229855	8524005- 74	TANTALUM, 330 MF ±20% 6 V
C2	222954	8524006- 70	TANTALUM, 220 MF ±20% 10 V
C3	54221	984003- 5	CERAMIC, 7-45 MMF 500 V
C4	225843	8524009- 93	TANTALUM, 47 MF ±20% 35 V
C5	229855	8524005- 74	TANTALUM, 330 MF ±20% 6 V
C6	224417	8524008-601	TANTALUM, 100 MF ±20% 20 V
C7	224417	8524008-601	TANTALUM, 100 MF ±20% 20 V
C8	229855	8524005- 74	TANTALUM, 330 MF ±20% 6 V
C9	300753	990786-165	PLASTIC, .015 MF ±10% 100 V
C10	269356	8524007- 66	TANTALUM, 150 MF ±20% 15 V
C11	223102	8983966- 1	CERAMIC, 0.1 MF 75 V
C12	227708	990786-171	PLASTIC, .047 MF ±10% 100 V
C13	227708	990786-171	PLASTIC, .047 MF ±10% 100 V
C14	225843	8524009- 93	TANTALUM, 47 MF ±20% 35 V
C15	225843	8524009- 93	TANTALUM, 47 MF ±20% 35 V

Symbol	Stock No.	Drawing No.	Description
C16	223672	990786-175	PLASTIC, 0.1 MF ±10% 100 V
C17	225606	993025-413	MICA, 10 MMF ±5% 100 V
C18	224417	8524008-601	TANTALUM, 100 MF ±20% 20 V
C19	226980	990786-163	PLASTIC, .01 MF ±10% 100 V
C20	226980	990786-163	PLASTIC, .01 MF ±10% 100 V
C21	223672	990786-175	PLASTIC, 0.1 MF ±10% 100 V
C22	223102	8983966- 1	CERAMIC, 0.1 MF 75 V
C23	222954	8524006- 70	TANTALUM, 220 MF ±20% 10 V
C24	108020	8959154-114	ELECTROLYTIC, 100 MF 25 V
C25	223672	990786-175	PLASTIC, 0.1 MF ±10% 100 V
C26	225609	993025-429	MICA, 47 MMF ±5% 100 V
C27	229873	8539993- 5	ELECTROLYTIC, 2000 MF 15 V
C28	229873	8539993- 5	ELECTROLYTIC, 2000 MF 15 V
C29	223670	8524008-171	TANTALUM, 4.7 MF ±20% 20 V
		-	
CR1	230511	8528891- 4	DIODE
CR2	230511	8528891- 4	DIODE
CR3 TO		-	
CR58	223687	8528891- 1	DIODE
CR59	230511	8528891- 4	DIODE
CR60	230511	8528891- 4	DIODE
CR61	230511	8528891- 4	DIODE
CR62	230511	8528891- 4	DIODE
CR63	229818	-	DIODE - TYPE 2N1933A
DL1	236206	8497121-502	DELAY LINE
P1	230446	8526621- 45	CONNECTOR - 32 PIN
Q1	229133	-	TRANSISTOR - TYPE 2N2189
Q2	227934	-	TRANSISTOR - TYPE 2N828
Q3	229133	-	TRANSISTOR - TYPE 2N2189
Q4	229133	-	TRANSISTOR - TYPE 2N2189
Q5	230464	-	TRANSISTOR - TYPE 2N2997
Q6	229133	-	TRANSISTOR - TYPE 2N2189
Q7	229133	-	TRANSISTOR - TYPE 2N2189
Q8	223684	-	TRANSISTOR - TYPE 2N1308
Q9	225598	-	TRANSISTOR - TYPE 2N1183
Q10	226685	-	TRANSISTOR - TYPE 2N2270
Q11	226685	-	TRANSISTOR - TYPE 2N2270
Q12	226685	-	TRANSISTOR - TYPE 2N2270
		-	
R1	502118	82283-141	180 OHMS ±5% 1/2 W
R2	222326	8868256- 41	VARIABLE, 500 OHMS 1/2 W
R3	236061	990476-293	FILM, 909 OHMS ±1% 1/2 W
R4	502291	82283-182	9100 OHMS ±5% 1/2 W
R5	502112	82283-137	120 OHMS ±5% 1/2 W
R6	502239	82283-173	3900 OHMS ±5% 1/2 W
R7	502133	82283-147	330 OHMS ±5% 1/2 W
R8	236055	990476-265	FILM, 464 OHMS ±1% 1/2 W
R9	512236	90496-172	3600 OHMS ±5% 1 W
R10	512230	90496-170	3000 OHMS ±5% 1 W
R11	235819	990476-449	FILM, 31,600 OHMS ±1% 1/2 W
R12	236090	990476-413	FILM, 13,300 OHMS ±1% 1/2 W
R13	230488	8980004-124	VARIABLE, 100 OHMS 1.0 W
R14	502111	82283-136	110 OHMS ±5% 1/2 W
R15	502022	82283-119	22 OHMS ±5% 1/2 W
R16	502022	82283-119	22 OHMS ±5% 1/2 W
R17	502022	82283-119	22 OHMS ±5% 1/2 W
R18	222326	8868256- 41	VARIABLE, 500 OHMS 1/2 W
R19	502118	82283-141	180 OHMS ±5% 1/2 W
R20	502275	82283-180	7500 OHMS ±5% 1/2 W
R21	236068	990476-325	FILM, 1780 OHMS ±1% 1/2 W
R22	502310	82283-183	10,000 OHMS ±5% 1/2 W
R23	502210	82283-159	1000 OHMS ±5% 1/2 W
R24	502110	82283-135	100 OHMS ±5% 1/2 W
R25	502110	82283-135	100 OHMS ±5% 1/2 W
R26	502320	82283-190	20,000 OHMS ±5% 1/2 W
R27	502210	82283-159	1000 OHMS ±5% 1/2 W
R28	502215	82283-163	1500 OHMS ±5% 1/2 W
R29	502168	82283-155	680 OHMS ±5% 1/2 W
R30	502218	82283-165	1800 OHMS ±5% 1/2 W
R31	502162	82283-154	620 OHMS ±5% 1/2 W
R32	502130	82283-122	30 OHMS ±5% 1/2 W
R33	236063	990476-305	FILM, 1100 OHMS ±1% 1/2 W

Symbol	Stock No.	Drawing No.	Description
R34	236063	990476-305	FILM, 1100 OHMS ±1% 1/2 W
R35	502320	82283-190	20,000 OHMS ±5% 1/2 W
R36	236059	990476-285	FILM, 750 OHMS ±1% 1/2 W
R37	236055	990476-265	FILM, 464 OHMS ±1% 1/2 W
R38	502110	82283-135	100 OHMS ±5% 1/2 W
R39	502230	82283-170	3000 OHMS ±5% 1/2 W
R40	502062	82283-130	62 OHMS ±5% 1/2 W
R41	502243	82283-174	4300 OHMS ±5% 1/2 W
R42	502239	82283-173	3900 OHMS ±5% 1/2 W
R43	502151	82283-152	510 OHMS ±5% 1/2 W
R44	502210	82283-159	1000 OHMS ±5% 1/2 W
R45	502210	82283-159	1000 OHMS ±5% 1/2 W
R46	502075	82283-132	75 OHMS ±5% 1/2 W
R47	502075	82283-132	75 OHMS ±5% 1/2 W
R48	236051	990476-185	FILM, 75 OHMS ±1% 1/2 W
R49	236051	990476-185	FILM, 75 OHMS ±1% 1/2 W
R50	236051	990476-185	FILM, 75 OHMS ±1% 1/2 W
R51	502216	82283-164	1600 OHMS ±5% 1/2 W
R52	502020	82283-118	20 OHMS ±5% 1/2 W
R53	236053	990476-247	FILM, 301 OHMS ±1% 1/2 W
		-	
TP1	214603	8941099- 4	JACK - TIP, YELLOW
TP2	214603	8941099- 4	JACK - TIP, YELLOW
TP3	214603	8941099- 4	JACK - TIP, YELLOW
		-	
		-	
		8543738-501	**CHROMA SEPARATOR MODULE (325/C13)**
		-	
C1	229873	8539993- 5	ELECTROLYTIC, 2000 MF 15 V
C2	217350	8959154-108	ELECTROLYTIC, 10 MF 25 V
C3	106552	8959154-184	ELECTROLYTIC, 250 MF 12 V
C4	230465	990786-173	PLASTIC, .068 MF ±10% 100 V
C5	106552	8959154-184	ELECTROLYTIC, 250 MF 12 V
C6	223672	990786-175	PLASTIC, 0.1 MF ±10% 100 V
C7	214738	8959154-194	ELECTROLYTIC, 20 MF 100 V
C8	260047	993025-442	MICA, 160 MMF ±5% 100 V
C9	106552	8959154-184	ELECTROLYTIC, 250 MF 12 V
C10	225611	993025-435	MICA, 82 MMF ±5% 100 V
C11	223247	8959154-417	ELECTROLYTIC, 200 MF 15 V
C12	225615	993025-441	MICA, 150 MMF ±5% 100 V
C13	229873	8539993- 5	ELECTROLYTIC, 2000 MF 15 V
C14	108020	8959154-114	ELECTROLYTIC, 100 MF 25 V
C15	219040	8959154-181	ELECTROLYTIC, 100 MF 12 V
C16	108020	8959154-114	ELECTROLYTIC, 100 MF 25 V
C17	300190	993025-453	MICA, 470 MMF ±5% 100 V
C18	217350	8959154-108	ELECTROLYTIC, 10 MF 25 V
C21	226980	990786-163	PLASTIC, .01 MF ±10% 100 V
C22	260051	993025-455	MICA, 560 MMF ±5% 100 V
C23	225620	993025-467	MICA, 1800 MMF ±5% 100 V
C24	219195	993025-461	MICA, 1000 MMF ±5% 100 V
C25	226102	993025-468	MICA, 2000 MMF ±5% 100 V
C26	226980	990786-163	PLASTIC, .01 MF ±10% 100 V
C27	219040	8959154-181	ELECTROLYTIC, 100 MF 12 V
C28	226980	990786-163	PLASTIC, .01 MF ±10% 100 V
C29	217350	8959154-108	ELECTROLYTIC, 10 MF 25 V
C30	300194	993025-459	MICA, 820 MMF ±5% 100 V
C31	300190	993025-453	MICA, 470 MMF ±5% 100 V
C32	225617	993025-452	MICA, 430 MMF ±5% 100 V
C33	219039	8959154-110	ELECTROLYTIC, 25 MF 25 V
C34	217350	8959154-108	ELECTROLYTIC, 10 MF 25 V
C35	217350	8959154-108	ELECTROLYTIC, 10 MF 25 V
C36	217350	8959154-108	ELECTROLYTIC, 10 MF 25 V
C37	217350	8959154-108	ELECTROLYTIC, 10 MF 25 V
C38	226980	990786-163	PLASTIC, .01 MF ±10% 100 V
C39	226980	990786-163	PLASTIC, .01 MF ±10% 100 V
C40	227708	990786-171	PLASTIC, .047 MF ±10% 100 V
C41	260049	993025-445	MICA, 220 MMF ±5% 100 V
C42	225614	993025-439	MICA, 120 MMF ±5% 100 V
C43	219040	8959154-181	ELECTROLYTIC, 100 MF 12 V
C44	108020	8959154-114	ELECTROLYTIC, 100 MF 25 V
C45	219195	993025-461	MICA, 1000 MMF ±5% 100 V
		-	

Symbol	Stock No.	Drawing No.	Description
CR1	225584	-	DIODE - TYPE 1N100A
CR3	225584	-	DIODE - TYPE 1N100A
CR4	226546	-	DIODE - TYPE 1N3063
CR5	225584	-	DIODE - TYPE 1N100A
CR6	225584	-	DIODE - TYPE 1N100A
L1	230486	8546652- 83	COIL - 7.5-18 MICROHENRY
L2	99792	8825473-506	COIL - 15 MICROHENRY
P1	230447	8526621- 46	CONNECTOR - 32 PIN
Q1	229133	-	TRANSISTOR - TYPE 2N2189
Q2	229133	-	TRANSISTOR - TYPE 2N2189
Q3	229133	-	TRANSISTOR - TYPE 2N2189
Q4	226685	-	TRANSISTOR - TYPE 2N2270
Q5	226441	-	TRANSISTOR - TYPE 2N1306
Q6	226441	-	TRANSISTOR - TYPE 2N1306
Q7	226441	-	TRANSISTOR - TYPE 2N1306
Q8	229133	-	TRANSISTOR - TYPE 2N2189
Q9	229133	-	TRANSISTOR - TYPE 2N2189
Q10	229133	-	TRANSISTOR - TYPE 2N2189
Q11	226685	-	TRANSISTOR - TYPE 2N2270
Q12	226441	-	TRANSISTOR - TYPE 2N1306
Q13	223685	-	TRANSISTOR - TYPE 2N1309
Q21	226685	-	TRANSISTOR - TYPE 2N2270
Q22 TO		-	
Q26	226442	-	TRANSISTOR - TYPE 2N1307
Q27	226441	-	TRANSISTOR - TYPE 2N1306
Q28	229133	-	TRANSISTOR - TYPE 2N2189
Q29	229133	-	TRANSISTOR - TYPE 2N2189
Q30	229133	-	TRANSISTOR - TYPE 2N2189
Q31	227934	-	TRANSISTOR - TYPE 2N828
Q32	226442	-	TRANSISTOR - TYPE 2N1307
Q33	226442	-	TRANSISTOR - TYPE 2N1307
Q34	229133	-	TRANSISTOR - TYPE 2N2189
Q35	229133	-	TRANSISTOR - TYPE 2N2189
Q36	229133	-	TRANSISTOR - TYPE 2N2189
Q37	229133	-	TRANSISTOR - TYPE 2N2189
Q38	226442	-	TRANSISTOR - TYPE 2N1307
		-	
R1	502315	82283-187	15,000 OHMS ±5% 1/2 W
R2	502111	82283-136	110 OHMS ±5% 1/2 W
R3	230488	8980004-124	VARIABLE, 100 OHMS 1 W
R4	502022	82283-119	22 OHMS ±5% 1/2 W
R5	236064	990476-309	FILM, 1210 OHMS ±1% 1/2 W
R6	502318	82283-189	18,000 OHMS ±5% 1/2 W
R7	236055	990476-265	FILM, 464 OHMS ±1% 1/2 W
R8	236064	990476-309	FILM, 1210 OHMS ±1% 1/2 W
R9	502318	82283-189	18,000 OHMS ±5% 1/2 W
R10	230487	8980004-127	VARIABLE, 1000 OHMS 1 W
R11	502210	82283-159	1000 OHMS ±5% 1/2 W
R12	502210	82283-159	1000 OHMS ±5% 1/2 W
R13	300374	90496-151	470 OHMS ±5% 1 W
R14	236051	990476-185	FILM, 75 OHMS ±1% 1/2 W
R15	502010	82283-111	10 OHMS ±5% 1/2 W
R16	502010	82283-111	10 OHMS ±5% 1/2 W
R17	502212	82283-161	1200 OHMS ±5% 1/2 W
R18	502120	82283-142	200 OHMS ±5% 1/2 W
R19	502310	82283-183	10,000 OHMS ±5% 1/2 W
R20	502382	82283-205	82,000 OHMS ±5% 1/2 W
R21	502215	82283-163	1500 OHMS ±5% 1/2 W
R22	502212	82283-161	1200 OHMS ±5% 1/2 W
R23	502282	82283-181	8200 OHMS ±5% 1/2 W
R24	502382	82283-205	82,000 OHMS ±5% 1/2 W
R25	502256	82283-177	5600 OHMS ±5% 1/2 W
R26	502110	82283-135	100 OHMS ±5% 1/2 W
R27	502336	82283-196	36,000 OHMS ±5% 1/2 W
R28	502175	82283-156	750 OHMS ±5% 1/2 W
R29	236066	990476-317	FILM, 1470 OHMS ±1% 1/2 W
R30	502322	82283-191	22,000 OHMS ±5% 1/2 W
R31	502256	82283-177	5600 OHMS ±5% 1/2 W
R32	236063	990476-305	FILM, 1100 OHMS ±1% 1/2 W
R33	236060	990476-289	FILM, 825 OHMS ±1% 1/2 W
R34	236056	990476-269	FILM, 511 OHMS ±1% 1/2 W
R35	502124	82283-144	240 OHMS ±5% 1/2 W

Symbol	Stock No.	Drawing No.	Description
R36	502022	82283-119	22 OHMS ±5% 1/2 W
R37	236051	990476-185	FILM, 75 OHMS ±1% 1/2 W
R38	502022	82283-119	22 OHMS ±5% 1/2 W
R39	502233	82283-171	3300 OHMS ±5% 1/2 W
R40	502175	82283-156	750 OHMS ±5% 1/2 W
R41	502175	82283-156	750 OHMS ±5% 1/2 W
R42	502220	82283-166	2000 OHMS ±5% 1/2 W
R43	502182	82283-157	820 OHMS ±5% 1/2 W
R44	502139	82283-149	390 OHMS ±5% 1/2 W
R45	502382	82283-205	82,000 OHMS ±5% 1/2 W
R46	502282	82283-181	8200 OHMS ±5% 1/2 W
R51	502268	82283-179	6800 OHMS ±5% 1/2 W
R52	502222	82283-167	2200 OHMS ±5% 1/2 W
R53	502222	82283-167	2200 OHMS ±5% 1/2 W
R54	502339	82283-197	39,000 OHMS ±5% 1/2 W
R55	502216	82283-164	1600 OHMS ±5% 1/2 W
R56	502275	82283-180	7500 OHMS ±5% 1/2 W
R57	502162	82283-154	620 OHMS ±5% 1/2 W
R58	502233	82283-171	3300 OHMS ±5% 1/2 W
R59	502212	82283-161	1200 OHMS ±5% 1/2 W
R60	502368	82283-203	68,000 OHMS ±5% 1/2 W
R61	502212	82283-161	1200 OHMS ±5% 1/2 W
R62	502315	82283-187	15,000 OHMS ±5% 1/2 W
R63	502212	82283-161	1200 OHMS ±5% 1/2 W
R64	502212	82283-161	1200 OHMS ±5% 1/2 W
R65	502233	82283-171	3300 OHMS ±5% 1/2 W
R66	502212	82283-161	1200 OHMS ±5% 1/2 W
R67	502310	82283-183	10,000 OHMS ±5% 1/2 W
R68	502243	82283-174	4300 OHMS ±5% 1/2 W
R69	502327	82283-193	27,000 OHMS ±5% 1/2 W
R70	502224	82283-168	2400 OHMS ±5% 1/2 W
R71	502243	82283-174	4300 OHMS ±5% 1/2 W
R72	502110	82283-135	100 OHMS ±5% 1/2 W
R73	502218	82283-165	1800 OHMS ±5% 1/2 W
R74	502175	82283-156	750 OHMS ±5% 1/2 W
R75	502333	82283-195	33,000 OHMS ±5% 1/2 W
R76	502282	82283-181	8200 OHMS ±5% 1/2 W
R78	502210	82283-159	1000 OHMS ±5% 1/2 W
R79	502210	82283-159	1000 OHMS ±5% 1/2 W
R80	502130	82283-146	300 OHMS ±5% 1/2 W
R81	502256	82283-177	5600 OHMS ±5% 1/2 W
R82	502210	82283-159	1000 OHMS ±5% 1/2 W
R83	502310	82283-183	10,000 OHMS ±5% 1/2 W
R84	232479	8980004-129	VARIABLE, 5000 OHMS 1 W
R85	502310	82283-183	10,000 OHMS ±5% 1/2 W
R86	502224	82283-168	2400 OHMS ±5% 1/2 W
R87	502220	82283-166	2000 OHMS ±5% 1/2 W
R88	236057	990476-277	FILM, 619 OHMS ±1% 1/2 W
R89	236057	990476-277	FILM, 619 OHMS ±1% 1/2 W
R90	502227	82283-169	2700 OHMS ±5% 1/2 W
R91	502227	82283-169	2700 OHMS ±5% 1/2 W
R92	502227	82283-169	2700 OHMS ±5% 1/2 W
R93	502151	82283-152	510 OHMS ±5% 1/2 W
R94	502251	82283-176	5100 OHMS ±5% 1/2 W
R95	502251	82283-176	5100 OHMS ±5% 1/2 W
R96	236057	990476-277	FILM, 619 OHMS ±1% 1/2 W
R97	236057	990476-277	FILM, 619 OHMS ±1% 1/2 W
R98	502210	82283-159	1000 OHMS ±5% 1/2 W
R99	502212	82283-161	1200 OHMS ±5% 1/2 W
R100	502215	82283-163	1500 OHMS ±5% 1/2 W
R101	502212	82283-161	1200 OHMS ±5% 1/2 W
R102	502224	82283-168	2400 OHMS ±5% 1/2 W
R103	502082	82283-133	82 OHMS ±5% 1/2 W
R104	502010	82283-111	10 OHMS ±5% 1/2 W
R105	502020	82283-118	20 OHMS ±5% 1/2 W
R106	232479	8980004-129	VARIABLE, 5000 OHMS 1 W
R107	502315	82283-187	15,000 OHMS ±5% 1/2 W
		-	
TP1	214603	8941099- 4	JACK - TIP, YELLOW
TP2	214603	8941099- 4	JACK - TIP, YELLOW
TP3	214603	8941099- 4	JACK - TIP, YELLOW
Z1	229087	-	QUAD - TYPE 2N4243

Symbol	Stock No.	Drawing No.	Description
		-	
		8543739-501	**COLOR ERROR DETECTOR MODULE (326/C14)**
		-	
C1	217350	8959154-108	ELECTROLYTIC, 10 MF 25 V
C2	230466	990786-174	PLASTIC, .082 MF ±10% 100 V
C3	230466	990786-174	PLASTIC, .082 MF ±10% 100 V
C4	219040	8959154-181	ELECTROLYTIC, 100 MF 12 V
C5	225614	993025-439	MICA, 120 MMF ±5% 100 V
C6	226980	990786-163	PLASTIC, .01 MF ±10% 100 V
C7	225614	993025-439	MICA, 120 MMF ±5% 100 V
C8	222954	8524006- 70	TANTALUM, 220 MF ±20% 10 V
C9	230466	990786-174	PLASTIC, .082 MF ±10% 100 V
C10	221890	8959154-101	ELECTROLYTIC, 1 MF 25 V
C11	226980	990786-163	PLASTIC, .01 MF ±10% 100 V
C12	226980	990786-163	PLASTIC, .01 MF ±10% 100 V
C13	226980	990786-163	PLASTIC, .01 MF ±10% 100 V
C14	225614	993025-439	MICA, 120 MMF ±5% 100 V
C15	230466	990786-174	PLASTIC, .082 MF ±10% 100 V
C16	226980	990786-163	PLASTIC, .01 MF ±10% 100 V
C17	226980	990786-163	PLASTIC, .01 MF ±10% 100 V
C18	108020	8959154-114	ELECTROLYTIC, 100 MF 25 V
C19	225614	993025-439	MICA, 120 MMF ±5% 100 V
C20	225611	993025-435	MICA, 82 MMF ±5% 100 V
C21	225611	993025-435	MICA, 82 MMF ±5% 100 V
C22	225614	993025-439	MICA, 120 MMF ±5% 100 V
C23	219040	8959154-181	ELECTROLYTIC, 100 MF 12 V
C24	225614	993025-439	MICA, 120 MMF ±5% 100 V
C25	225614	993025-439	MICA, 120 MMF ±5% 100 V
C26	225609	993025-429	MICA, 47 MMF ±5% 100 V
C27	300443	993025-446	MICA, 240 MMF ±5% 100 V
C28	225609	993025-429	MICA, 47 MMF ±5% 100 V
C29	230466	990786-174	PLASTIC, .082 MF ±10% 100 V
C30	225613	993025-437	MICA, 100 MMF ±5% 100 V
C31	225607	993025-423	MICA, 27 MMF ±5% 100 V
C40	217350	8959154-108	ELECTROLYTIC, 10 MF 25 V
C41	217350	8959154-108	ELECTROLYTIC, 10 MF 25 V
C42	217350	8959154-108	ELECTROLYTIC, 10 MF 25 V
C43	230466	990786-174	PLASTIC, .082 MF ±10% 100 V
C44	230484	8524006- 51	TANTALUM, 33 MF ±20% 10 V
C45	222954	8524006- 70	TANTALUM, 220 MF ±20% 10 V
C46	219040	8959154-181	ELECTROLYTIC, 100 MF 12 V
C47	219040	8959154-181	ELECTROLYTIC, 100 MF 12 V
C48	225614	993025-439	MICA, 120 MMF ±5% 100 V
C49	260045	993025-427	MICA, 39 MMF ±5% 100 V
C50	225611	993025-435	MICA, 82 MMF ±5% 100 V
C51	225610	993025-434	MICA, 75 MMF ±5% 100 V
C52	260045	993025-427	MICA, 39 MMF ±5% 100 V
C53	214738	8959154-194	ELECTROLYTIC, 20 MF 100 V
C54	230466	990786-174	PLASTIC, .082 MF ±10% 100 V
C55	230466	990786-174	PLASTIC, .082 MF ±10% 100 V
C56	226645	8524008- 79	TANTALUM, 10 MF ±20% 20 V
C57	226645	8524008- 79	TANTALUM, 10 MF ±20% 20 V
C58	225619	993025-466	MICA, 1600 MMF ±5% 100 V
C59	223672	990786-175	PLASTIC, 0.1 MF ±10% 100 V
C60	225611	993025-435	MICA, 82 MMF ±5% 100 V
C61	225609	993025-429	MICA, 47 MMF ±5% 100 V
C62	225613	993025-437	MICA, 100 MMF ±5% 100 V
C63	300182	993025-432	MICA, 62 MMF ±5% 100 V
C64	217350	8959154-108	ELECTROLYTIC, 10 MF 25 V
C65	221890	8959154-101	ELECTROLYTIC, 1 MF 25 V
C66	226980	990786-163	PLASTIC, .01 MF ±10% 100 V
C67	226980	990786-163	PLASTIC, .01 MF ±10% 100 V
C68	226980	990786-163	PLASTIC, .01 MF ±10% 100 V
C69	226980	990786-163	PLASTIC, .01 MF ±10% 100 V
C70	108020	8959154-114	ELECTROLYTIC, 100 MF 25 V
C71	226980	990786-163	PLASTIC, .01 MF ±10% 100 V
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CR1	226546	-	DIODE - TYPE 1N3063
CR2	226546	-	DIODE - TYPE 1N3063
CR3	229818	-	DIODE - TYPE 1N1933A
CR4	218501	8983872- 1	DIODE

Symbol	Stock No.	Drawing No.	Description
CR5 TO		-	
CR13	226546	-	DIODE - TYPE 1N3063
CR14	225314	-	DIODE - TYPE 1N3016B
CR15	226546	-	DIODE - TYPE 1N3063
CR16	226546	-	DIODE - TYPE 1N3063
CR17	218501	8983872- 1	DIODE
CR18	226546	-	DIODE - TYPE 1N3063
CR25		-	
TO		-	
CR31	226546	-	DIODE - TYPE 1N3063
CR32	229818	-	DIODE - TYPE 1N1933A
CR33	226546	-	DIODE - TYPE 1N3063
CR34	218501	8983872- 1	DIODE
CR35	226546	-	DIODE - TYPE 1N3063
DL1	230514	8548697- 1	DELAY LINE
L1	205878	8825473-502	COIL - RF CHOKE, 4 MICROHENRY
L2	209148	8825473-501	COIL - RF CHOKE, 2 MICROHENRY
L3	230938	8545694- 27	COIL - RF CHOKE, 15 MICROHENRY
L4	230486	8546652- 83	COIL - RF CHOKE, 7.5 TO 18 MICROHENRY
L5	205878	8825473-502	COIL - RF CHOKE, 4 MICROHENRY
L6	202910	8825473-505	COIL - RF CHOKE, 10 MICROHENRY
L7	209148	8825473-501	COIL - RF CHOKE, 2 MICROHENRY
L8	202910	8825473-505	COIL - RF CHOKE, 10 MICROHENRY
L9	230939	8545694- 30	COIL - RF CHOKE, 27 MICROHENRY
L15	99792	8825473-506	COIL - RF CHOKE, 15 MICROHENRY
L16	205518	8825473-507	COIL - RF CHOKE, 20 MICROHENRY
L17	202910	8825473-505	COIL - RF CHOKE, 10 MICROHENRY
L18	202910	8825473-505	COIL - RF CHOKE, 10 MICROHENRY
L19	210343	8825473-503	COIL - RF CHOKE, 6 MICROHENRY
L20	99792	8825473-506	COIL - RF CHOKE, 15 MICROHENRY
P1	230448	8526621- 47	CONNECTOR - 32 PIN
Q1	227934	-	TRANSISTOR - TYPE 2N828
Q2	227934	-	TRANSISTOR - TYPE 2N828
Q3	227934	-	TRANSISTOR - TYPE 2N828
Q4	227934	-	TRANSISTOR - TYPE 2N828
Q5 TO		-	
Q9	227000	-	TRANSISTOR - TYPE 2N708
Q10	229133	-	TRANSISTOR - TYPE 2N2189
Q11	229133	-	TRANSISTOR - TYPE 2N2189
Q12	229133	-	TRANSISTOR - TYPE 2N2189
Q13	229133	-	TRANSISTOR - TYPE 2N2189
Q14	227934	-	TRANSISTOR - TYPE 2N828
Q15	229820	-	TRANSISTOR - TYPE 2N967
Q16	227934	-	TRANSISTOR - TYPE 2N828
Q17	227000	-	TRANSISTOR - TYPE 2N708
Q18	227934	-	TRANSISTOR - TYPE 2N828
Q19	227934	-	TRANSISTOR - TYPE 2N828
Q20	227934	-	TRANSISTOR - TYPE 2N828
Q21	229820	-	TRANSISTOR - TYPE 2N967
Q22	229820	-	TRANSISTOR - TYPE 2N967
Q23	229820	-	TRANSISTOR - TYPE 2N967
Q24	229820	-	TRANSISTOR - TYPE 2N967
Q25	227934	-	TRANSISTOR - TYPE 2N828
Q26	227934	-	TRANSISTOR - TYPE 2N828
Q30	226238	-	TRANSISTOR - TYPE 2N1319
Q31	226441	-	TRANSISTOR - TYPE 2N1306
Q32	226685	-	TRANSISTOR - TYPE 2N2270
Q33	229133	-	TRANSISTOR - TYPE 2N2189
Q34	223684	-	TRANSISTOR - TYPE 2N1308
Q35	223684	-	TRANSISTOR - TYPE 2N1308
Q36	227934	-	TRANSISTOR - TYPE 2N828
Q37	229820	-	TRANSISTOR - TYPE 2N967
Q38	227000	-	TRANSISTOR - TYPE 2N708
Q39	227934	-	TRANSISTOR - TYPE 2N828
Q40	229820	-	TRANSISTOR - TYPE 2N967
Q41	227000	-	TRANSISTOR - TYPE 2N708
Q42	227934	-	TRANSISTOR - TYPE 2N828
Q43	225373	-	TRANSISTOR - TYPE 2N929
Q44	227000	-	TRANSISTOR - TYPE 2N708
Q45	227000	-	TRANSISTOR - TYPE 2N708
Q46	227000	-	TRANSISTOR - TYPE 2N708
Q47	229820	-	TRANSISTOR - TYPE 2N967

Symbol	Stock No.	Drawing No.	Description
Q48	227934	-	TRANSISTOR - TYPE 2N828
Q49	227934	-	TRANSISTOR - TYPE 2N828
Q50	227000	-	TRANSISTOR - TYPE 2N708
Q51	227000	-	TRANSISTOR - TYPE 2N708
Q52	227000	-	TRANSISTOR - TYPE 2N708
Q53	227000	-	TRANSISTOR - TYPE 2N708
Q54	229133	-	TRANSISTOR - TYPE 2N2189
		-	
R1	502220	82283-166	2000 OHMS ±5% 1/2 W
R2	502210	82283-159	1000 OHMS ±5% 1/2 W
R3	502210	82283-159	1000 OHMS ±5% 1/2 W
R4	502147	82283-151	470 OHMS ±5% 1/2 W
R5	502310	82283-183	10,000 OHMS ±5% 1/2 W
R6	502130	82283-146	300 OHMS ±5% 1/2 W
R7	502120	82283-142	200 OHMS ±5% 1/2 W
R8	502333	82283-195	33,000 OHMS ±5% 1/2 W
R9	502120	82283-142	200 OHMS ±5% 1/2 W
R10	502262	82283-178	6200 OHMS ±5% 1/2 W
R11	502275	82283-180	7500 OHMS ±5% 1/2 W
R12	502220	82283-166	2000 OHMS ±5% 1/2 W
R13	502262	82283-178	6200 OHMS ±5% 1/2 W
R14	502212	82283-161	1200 OHMS ±5% 1/2 W
R15	522233	99126-171	3300 OHMS ±5% 2 W
R16	502212	82283-161	1200 OHMS ±5% 1/2 W
R17	502168	82283-131	68 OHMS ±5% 1/2 W
R19	502136	82283-148	360 OHMS ±5% 1/2 W
R20	502215	82283-163	1500 OHMS ±5% 1/2 W
R21	502110	82283-135	100 OHMS ±5% 1/2 W
R22	502210	82283-159	1000 OHMS ±5% 1/2 W
R23	502210	82283-159	1000 OHMS ±5% 1/2 W
R24	502162	82283-154	620 OHMS ±5% 1/2 W
R25	502233	82283-171	3300 OHMS ±5% 1/2 W
R26	502251	82283-176	5100 OHMS ±5% 1/2 W
R27	502224	82283-168	2400 OHMS ±5% 1/2 W
R28	502230	82283-170	3000 OHMS ±5% 1/2 W
R29	502318	82283-189	18,000 OHMS ±5% 1/2 W
R30	502320	82283-190	20,000 OHMS ±5% 1/2 W
R31	502220	82283-166	2000 OHMS ±5% 1/2 W
R32	502162	82283-154	620 OHMS ±5% 1/2 W
R33	502347	82283-199	47,000 OHMS ±5% 1/2 W
R34	502236	82283-172	3600 OHMS ±5% 1/2 W
R35	502020	82283-118	20 OHMS ±5% 1/2 W
R36	502222	82283-167	2200 OHMS ±5% 1/2 W
R37	502375	82283-204	75,000 OHMS ±5% 1/2 W
R38	502147	82283-151	470 OHMS ±5% 1/2 W
R39	502333	82283-195	33,000 OHMS ±5% 1/2 W
R40	502113	82283-138	130 OHMS ±5% 1/2 W
R41	502147	82283-151	470 OHMS ±5% 1/2 W
R42	502147	82283-151	470 OHMS ±5% 1/2 W
R43	502147	82283-151	470 OHMS ±5% 1/2 W
R44	502210	82283-159	1000 OHMS ±5% 1/2 W
R45	502322	82283-191	22,000 OHMS ±5% 1/2 W
R46	502368	82283-203	68,000 OHMS ±5% 1/2 W
R47	502147	82283-151	470 OHMS ±5% 1/2 W
R48	502218	82283-165	1800 OHMS ±5% 1/2 W
R49	502147	82283-151	470 OHMS ±5% 1/2 W
R50	502222	82283-167	2200 OHMS ±5% 1/2 W
R51	502375	82283-204	75,000 OHMS ±5% 1/2 W
R52	502147	82283-151	470 OHMS ±5% 1/2 W
R53	502310	82283-183	10,000 OHMS ±5% 1/2 W
R54	502222	82283-167	2200 OHMS ±5% 1/2 W
R55	502375	82283-204	75,000 OHMS ±5% 1/2 W
R156	502122	82283-143	220 OHMS ±5% 1/2 W
R57	502213	82283-162	1300 OHMS ±5% 1/2 W
R58	502422	82283-215	220,000 OHMS ±5% 1/2 W
R59	502256	82283-177	5600 OHMS ±5% 1/2 W
R60	502422	82283-215	220,000 OHMS ±5% 1/2 W
R61	502213	82283-162	1300 OHMS ±5% 1/2 W
R62	502122	82283-143	220 OHMS ±5% 1/2 W
R63	502415	82283-211	150,000 OHMS ±5% 1/2 W
R64	502310	82283-183	10,000 OHMS ±5% 1/2 W
R65	502233	82283-171	3300 OHMS ±5% 1/2 W

Symbol	Stock No.	Drawing No.	Description
R66	502210	82283-159	1000 OHMS ±5% 1/2 W
R67	502147	82283-151	470 OHMS ±5% 1/2 W
R68	502020	82283-118	20 OHMS ±5% 1/2 W
R69	502020	82283-118	20 OHMS ±5% 1/2 W
R70	502062	82283-130	62 OHMS ±5% 1/2 W
R71	502343	82283-198	43,000 OHMS ±5% 1/2 W
R72	502212	82283-161	1200 OHMS ±5% 1/2 W
R73	502233	82283-171	3300 OHMS ±5% 1/2 W
R74	502268	82283-179	6800 OHMS ±5% 1/2 W
R90	502415	82283-211	150,000 OHMS ±5% 1/2 W
R91	502310	82283-183	10,000 OHMS ±5% 1/2 W
R92	502312	82283-185	12,000 OHMS ±5% 1/2 W
R93	502036	82283-124	36 OHMS ±5% 1/2 W
R94	230488	8980004-124	VARIABLE, 100 OHMS 1 W
R95	502168	82283-155	680 OHMS ±5% 1/2 W
R96	502210	82283-159	1000 OHMS ±5% 1/2 W
R97	502233	82283-171	3300 OHMS ±5% 1/2 W
R98	502227	82283-169	2700 OHMS ±5% 1/2 W
R99	502336	82283-196	36,000 OHMS ±5% 1/2 W
R100	502251	82283-176	5100 OHMS ±5% 1/2 W
R101	502268	82283-179	6800 OHMS ±5% 1/2 W
R102	502262	82283-178	6200 OHMS ±5% 1/2 W
R103	502213	82283-162	1300 OHMS ±5% 1/2 W
R104	502233	82283-171	3300 OHMS ±5% 1/2 W
R105	502215	82283-163	1500 OHMS ±5% 1/2 W
R106	502075	82283-132	75 OHMS ±5% 1/2 W
R107	502022	82283-119	22 OHMS ±5% 1/2 W
R108	502020	82283-118	20 OHMS ±5% 1/2 W
R109	502218	82283-165	1800 OHMS ±5% 1/2 W
R110	502368	82283-203	68,000 OHMS ±5% 1/2 W
R111	502147	82283-151	470 OHMS ±5% 1/2 W
R112	502147	82283-151	470 OHMS ±5% 1/2 W
R113	502113	82283-138	130 OHMS ±5% 1/2 W
R114	502333	82283-195	33,000 OHMS ±5% 1/2 W
R115	502147	82283-151	470 OHMS ±5% 1/2 W
R116	502147	82283-151	470 OHMS ±5% 1/2 W
R117	502318	82283-189	18,000 OHMS ±5% 1/2 W
R118	502147	82283-151	470 OHMS ±5% 1/2 W
R119	502251	82283-176	5100 OHMS ±5% 1/2 W
R120	502147	82283-151	470 OHMS ±5% 1/2 W
R121	502210	82283-159	1000 OHMS ±5% 1/2 W
R122	502147	82283-151	470 OHMS ±5% 1/2 W
R123	502210	82283-159	1000 OHMS ±5% 1/2 W
R124	502147	82283-151	470 OHMS ±5% 1/2 W
R125	502343	82283-198	43,000 OHMS ±5% 1/2 W
R126	502147	82283-151	470 OHMS ±5% 1/2 W
R127	502110	82283-135	100 OHMS ±5% 1/2 W
R128	502210	82283-159	1000 OHMS ±5% 1/2 W
R129	502210	82283-159	1000 OHMS ±5% 1/2 W
R130	502320	82283-190	20,000 OHMS ±5% 1/2 W
R131	502320	82283-190	20,000 OHMS ±5% 1/2 W
R132	229880	8980004-125	VARIABLE, 200 OHMS 1 W
R133	502122	82283-119	22 OHMS ±5% 1/2 W
R134	502122	82283-119	22 OHMS ±5% 1/2 W
R135	502510	82283-231	1 MEGOHM ±5% 1/2 W
R136	522233	99126-171	3300 OHMS ±5% 2 W
R137	502210	82283-159	1000 OHMS ±5% 1/2 W
R138	502247	82283-175	4700 OHMS ±5% 1/2 W
R139	502210	82283-159	1000 OHMS ±5% 1/2 W
R140	502175	82283-156	750 OHMS ±5% 1/2 W
R141	502130	82283-146	300 OHMS ±5% 1/2 W
R142	502375	82283-204	75,000 OHMS ±5% 1/2 W
R143	68945	8971860-914	VARIABLE, 100,000 OHMS 2 W
R144	502110	82283-135	100 OHMS ±5% 1/2 W
R145	502318	82283-189	18,000 OHMS ±5% 1/2 W
R146	502147	82283-151	470 OHMS ±5% 1/2 W
R147	502210	82283-159	1000 OHMS ±5% 1/2 W
R148	502368	82283-203	68,000 OHMS ±5% 1/2 W
R149	502368	82283-203	68,000 OHMS ±5% 1/2 W
R150	502147	82283-151	470 OHMS ±5% 1/2 W
R151	502310	82283-183	10,000 OHMS ±5% 1/2 W
R152	502262	82283-178	6200 OHMS ±5% 1/2 W

Symbol	Stock No.	Drawing No.	Description
R153	502212	82283-161	1200 OHMS ±5% 1/2 W
R154	502220	82283-166	2000 OHMS ±5% 1/2 W
R155	502251	82283-176	5100 OHMS ±5% 1/2 W
R156	502051	82283-128	51 OHMS ±5% 1/2 W
R157	502213	82283-162	1300 OHMS ±5% 1/2 W
R158	502136	82283-148	360 OHMS ±5% 1/2 W
R159	502122	82283-143	220 OHMS ±5% 1/2 W
R160	502168	82283-155	680 OHMS ±5% 1/2 W
R161	502210	82283-159	1000 OHMS ±5% 1/2 W
R162	502210	82283-159	1000 OHMS ±5% 1/2 W
R163	502318	82283-189	18,000 OHMS ±5% 1/2 W
R164	502127	82283-145	270 OHMS ±5% 1/2 W
R165	502239	82283-173	3900 OHMS ±5% 1/2 W
R166	502415	82283-211	150,000 OHMS ±5% 1/2 W
R167	502075	82283-132	75 OHMS ±5% 1/2 W
R168	502020	82283-118	20 OHMS ±5% 1/2 W
R169	502215	82283-163	1500 OHMS ±5% 1/2 W
R170	236105	99206-263	22 MEGOHMS ±5% 1/4 W
R171	232479	8980004-129	VARIABLE, 5000 OHMS 1 W
		-	
T1	230485	8535705- 2	TRANSFORMER
TP1	214603	8941099- 4	JACK - TIP, YELLOW
TP2	214603	8941099- 4	JACK - TIP, YELLOW
TP3	214603	8941099- 4	JACK - TIP, YELLOW
		-	
		-	
		-	
		-	**MI-40688 FIXED DELAY LINE ASSEMBLY (MONO/COLOR) FOR TR-22**
		-	
		-	
		-	
		-	
	502182	82283-157	RESISTOR - 820 OHMS ±5% 1/2 W
		-	
		-	
		8766936-501	FIXED DELAY LINE ASSEMBLY (MONO/COLOR ATC)
		-	
	51800	1510021-111	CONNECTOR
		-	
		8545704-501	BOARD ASSEMBLY
		-	
C1	255030	993025-844	MICA, 200 MMF ±1% 100 V
C2 TO		-	
C58	223551	993025-854	MICA, 510 MMF ±1% 100 V
C59	255030	993025-844	MICA, 200 MMF ±1% 100 V
C60	213496	993025-629	MICA, 47 MMF ±2% 100 V
C61	226102	993025-468	MICA, 2000 MMF ±5% 100 V
		-	
L1 TO		-	
L58	229875	8540908- 3	COIL
L59	229876	8546616- 3	COIL - VARIABLE, 5-9 MICROHENRY
		-	
R1	233505	1510136-245	FILM, 287 OHMS ±1% 1/2 W
R2	231712	1510136-185	FILM, 75 OHMS ±1% 1/2 W
R3	229825	1510136-129	FILM, 19.6 OHMS ±1% 1/2 W
R4	230885	8868256- 39	VARIABLE, 100 OHMS ±20% 1/2 W
R5	502110	82283-135	100 OHMS ±5% 1/2 W
R6	234461	1510136-226	FILM, 182 OHMS ±1% 1/4 W
R7	231712	1510136-185	FILM, 75 OHMS ±1% 1/2 W
		-	
		-	
		-	
		-	**MI-43392 FIXED DELAY LINE MODULE—ATC (3A2/3A3) FOR TR-3, TR-4**
		-	
		-	
		-	
		-	
		8549757-501	MODULE - FIXED DELAY LINE
		-	
C1	255030	993025-844	MICA, 200 MMF ±1% 100 V
C2 TO		-	
C59	223551	993025-854	MICA, 510 MMF ±1% 100 V

Symbol	Stock No.	Drawing No.	Description
C60	213496	993025-629	MICA, 47 MMF ±2% 100 V
C61	226102	993025-468	MICA, 2000 MMF ±5% 100 V
C62	255030	993025-844	MICA, 200 MMF ±1% 100 V
C63	234460	993025-870	MICA, 2400 MMF ±1% 100 V
C64	921309	993025-839	MICA, 120 MMF ±1% 100 V
C65	921309	993025-839	MICA, 120 MMF ±1% 100 V
C66	234460	993025-870	MICA, 2400 MMF ±1% 100 V
C67	234459	993025-836	MICA, 91 MMF ±1% 100 V
		-	
L1 TO		-	
L58	232779	8540908- 5	COIL - 2.6 MICROHENRY
L59	229876	8546616- 3	COIL - VARIABLE, 5-9 MICROHENRY
L60	232779	8540908- 5	COIL - 2.6 MICROHENRY
L61		8540908- 6	COIL - 7.1 MICROHENRY
L62		3310282- 1	COIL - 0.5 MICROHENRY
		-	
R1	233505	1510136-245	FILM, 287 OHMS ±1% 1/4 W
R2	231712	1510136-185	FILM, 75 OHMS ±1% 1/4 W
R3	229825	1510136-129	FILM, 19.6 OHMS ±1% 1/4 W
R4	230885	8868256- 39	VARIABLE, 100 OHMS 1/2 W
R5	502110	82283-135	100 OHMS ±5% 1/2 W
R6	234461	1510136-226	FILM, 182 OHMS ±1% 1/4 W
R7	231712	1510136-185	FILM, 75 OHMS ±1% 1/4 W

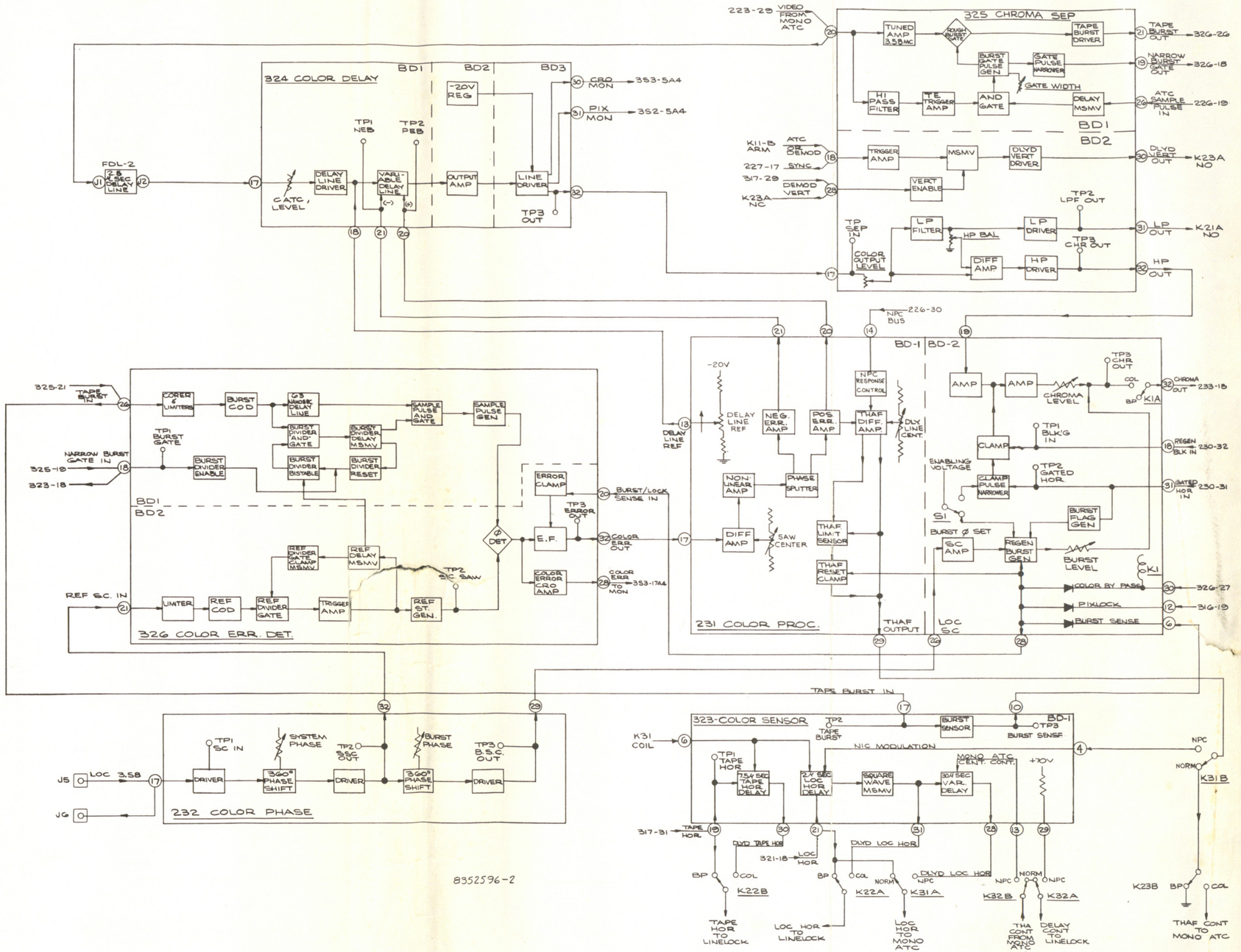
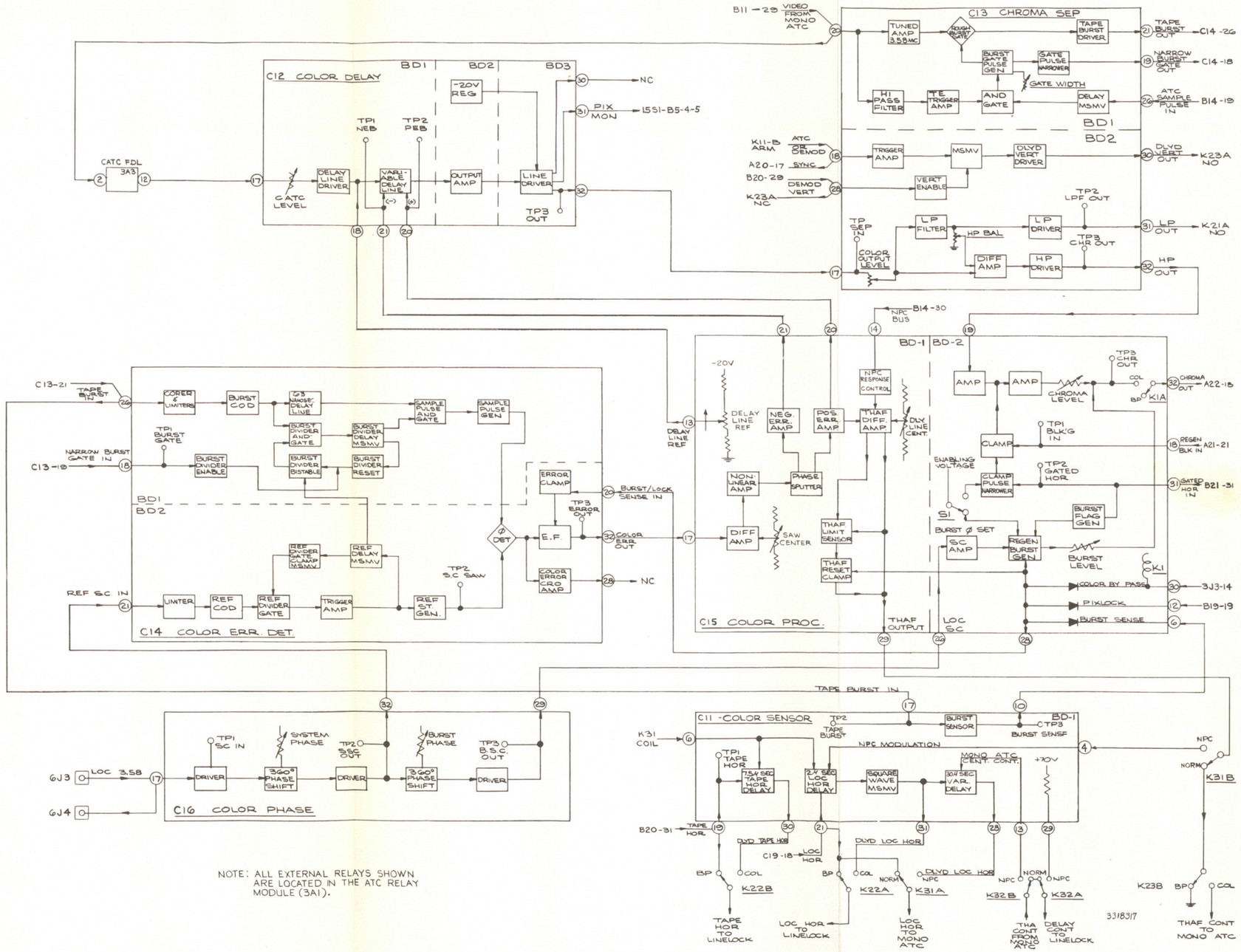


Figure 78—Color ATC Functional Diagram for TR-22 Machines



NOTE: ALL EXTERNAL RELAYS SHOWN ARE LOCATED IN THE ATC RELAY MODULE (3A1).

Figure 79—Color ATC Functional Diagram for TR-3/TR-4 Machines

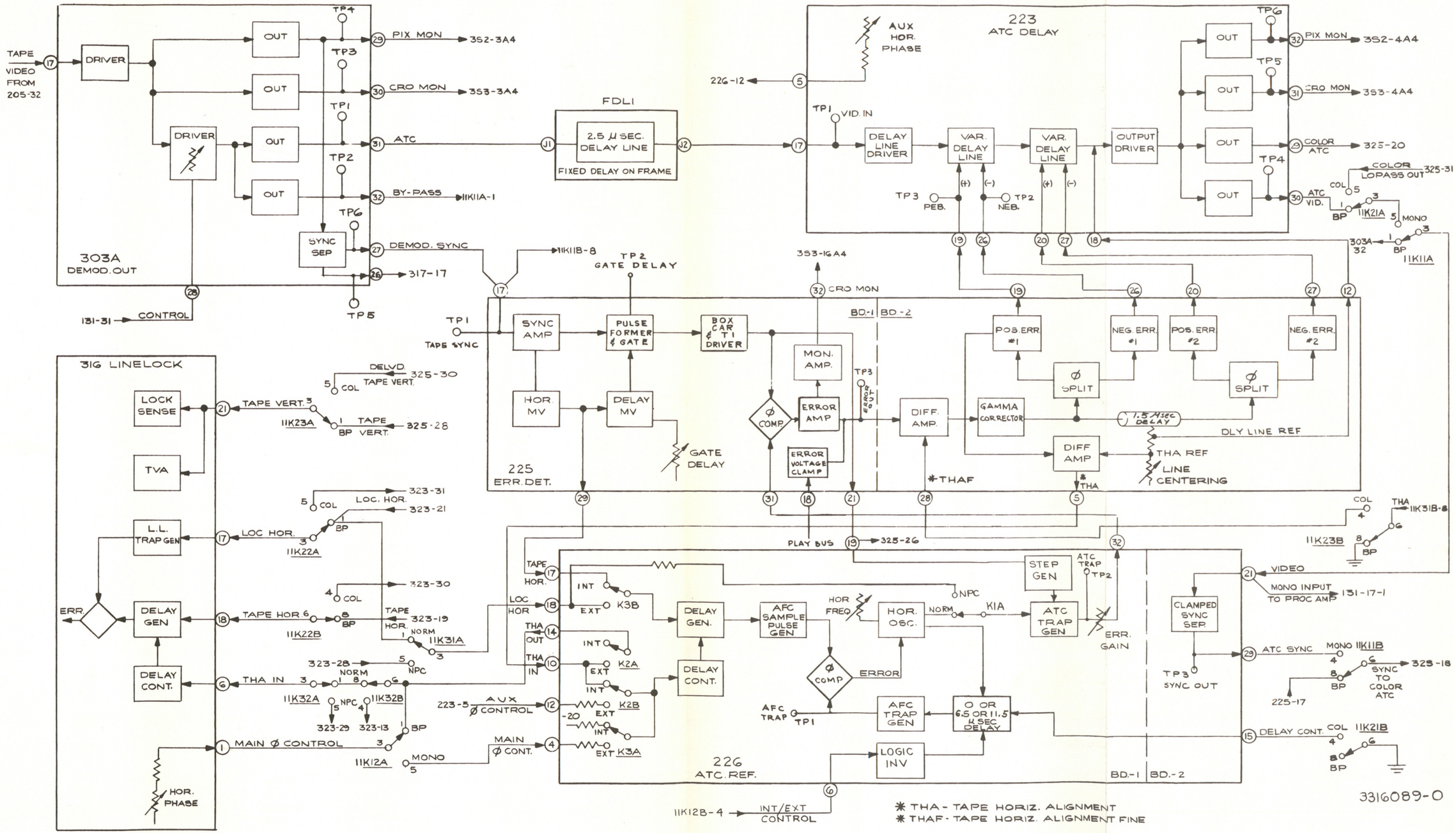


Figure 80—Monochrome ATC Functional Diagram for TR-22 Machines

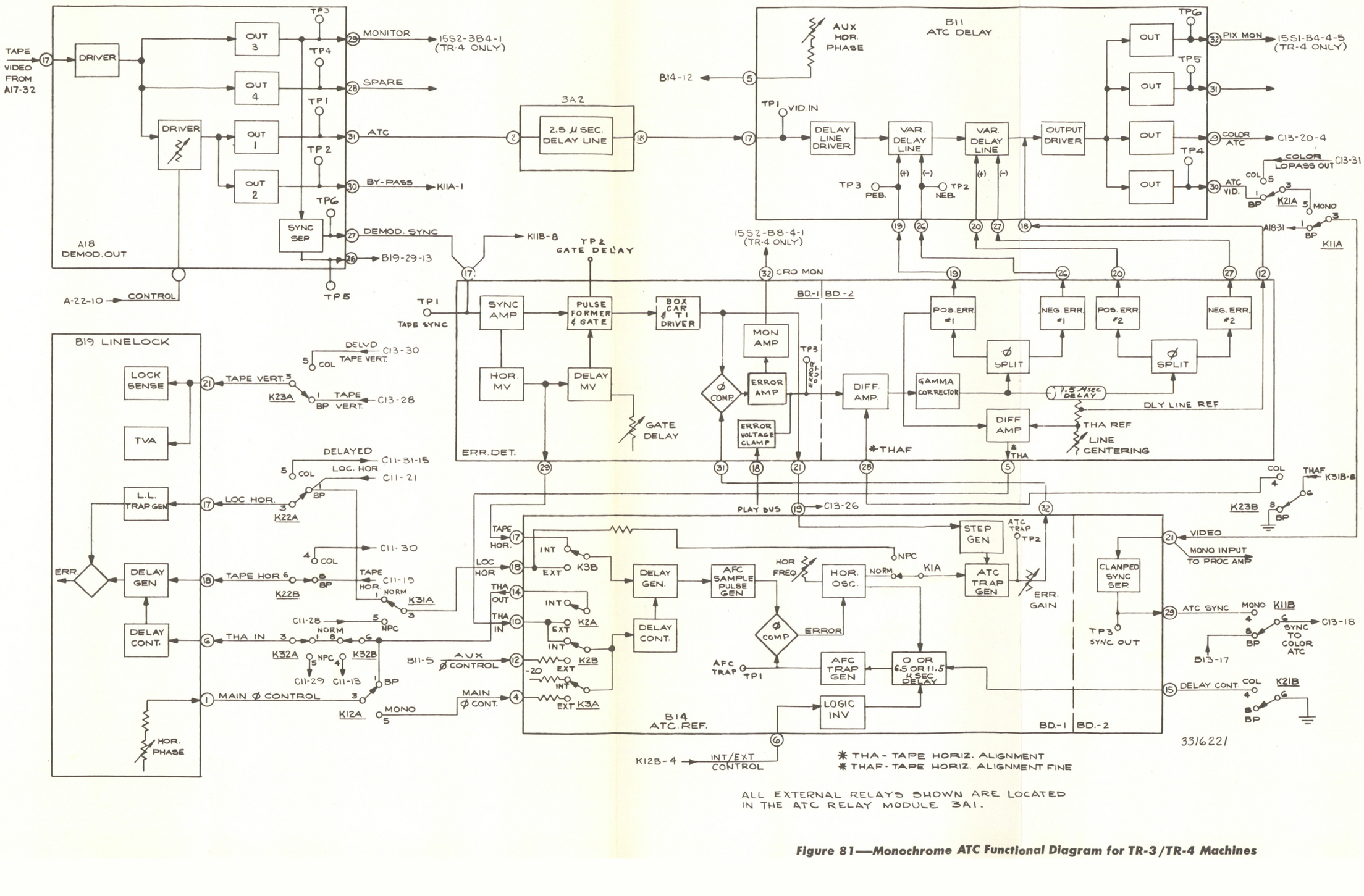


Figure 81—Monochrome ATC Functional Diagram for TR-3/TR-4 Machines

Figure 82—ATC Control Functional Diagram for TR-22 Machines

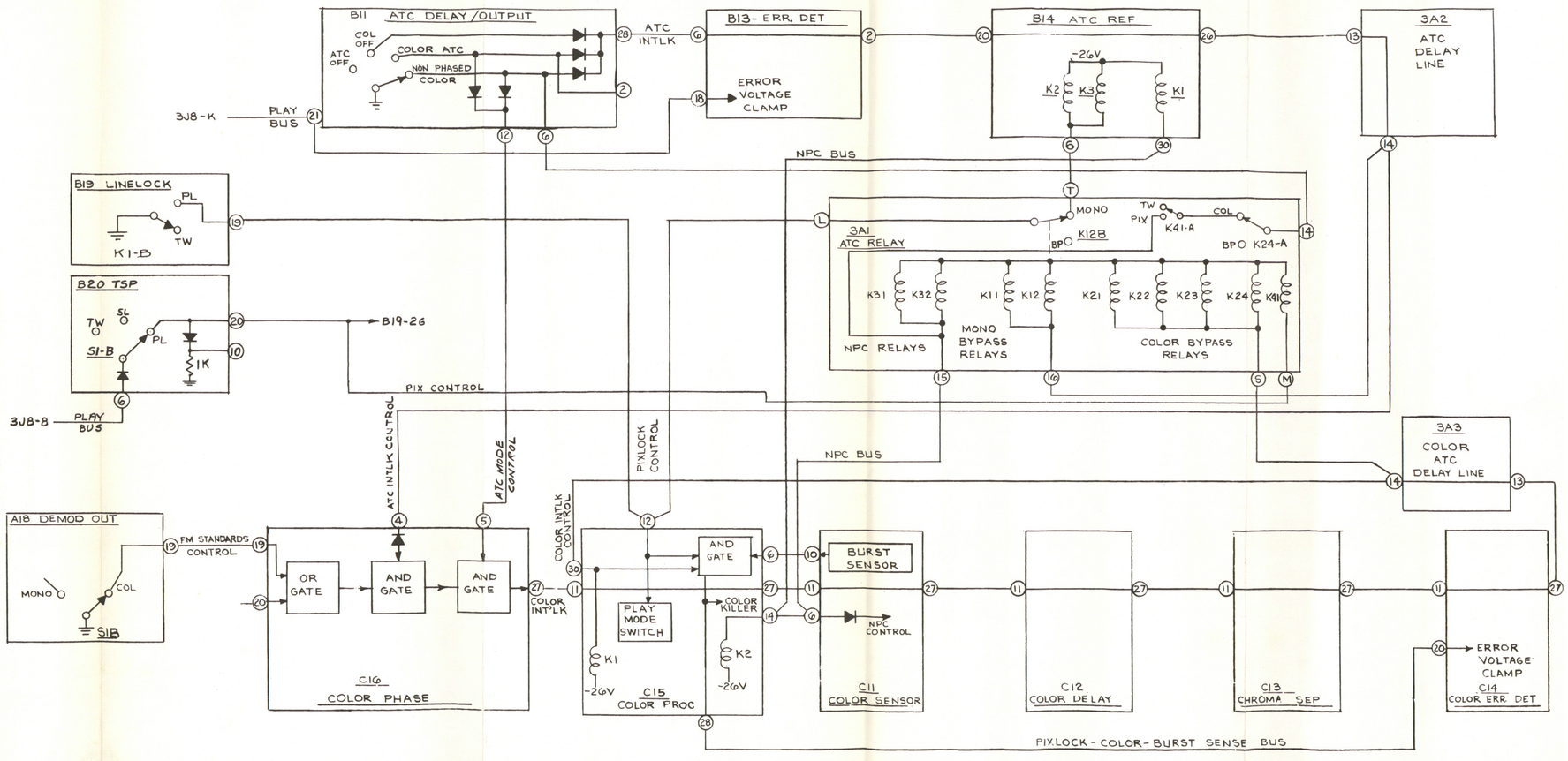
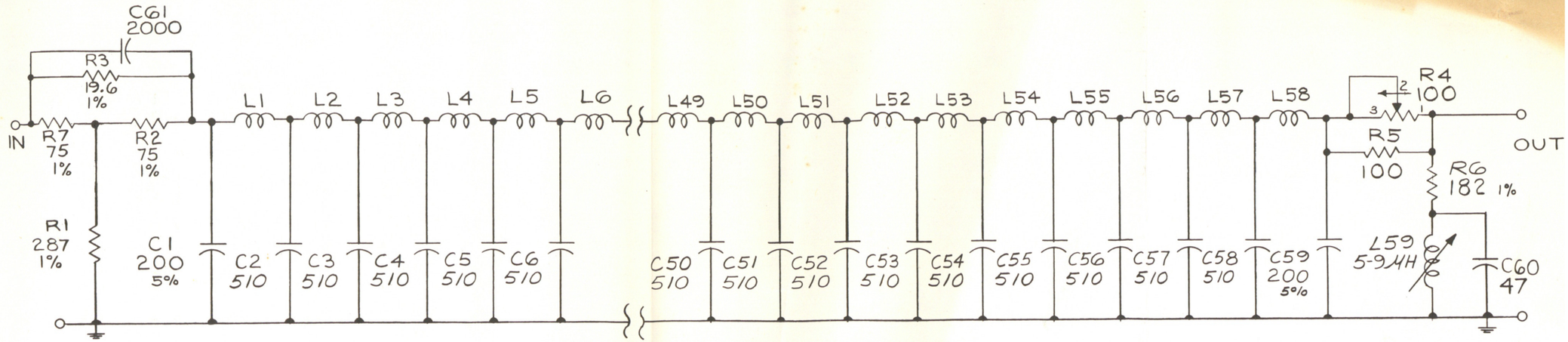
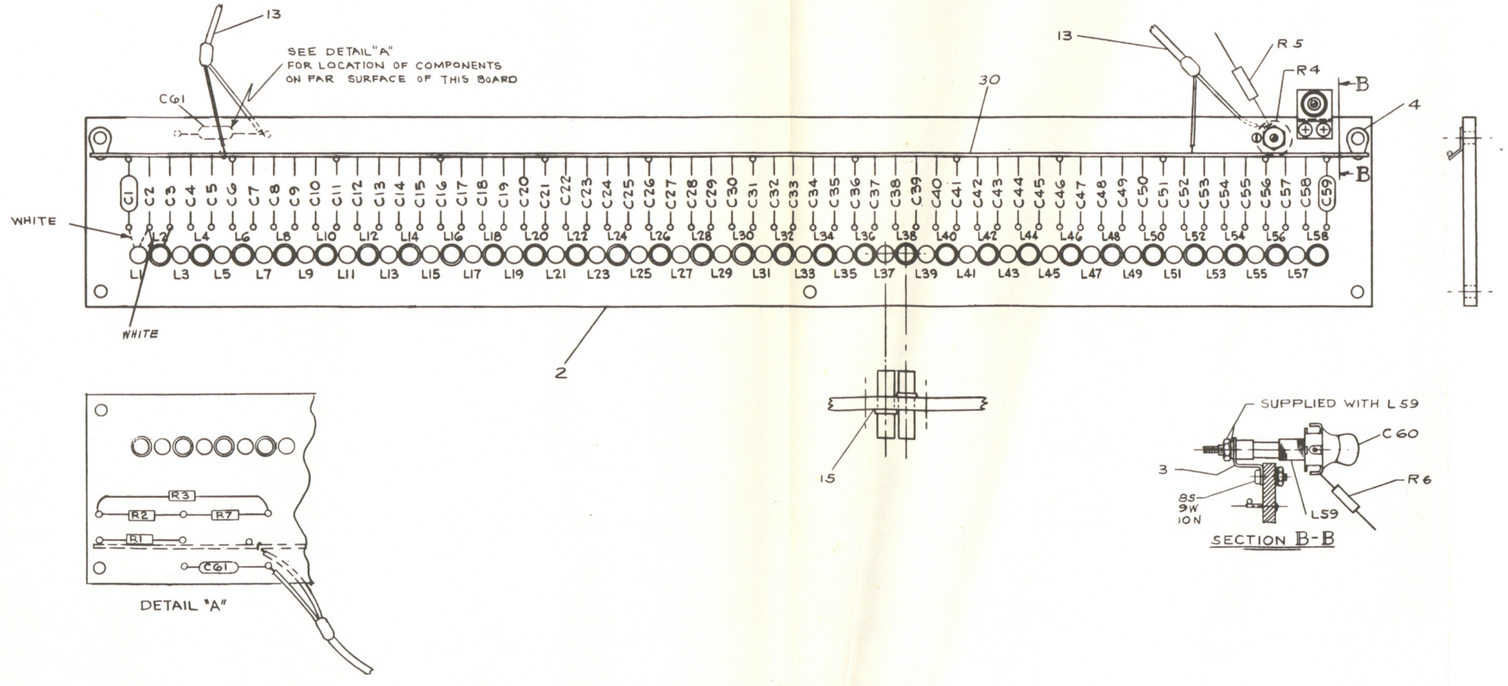


Figure 83—ATC Control Functional Diagram for TR-3/TR-4 Machines

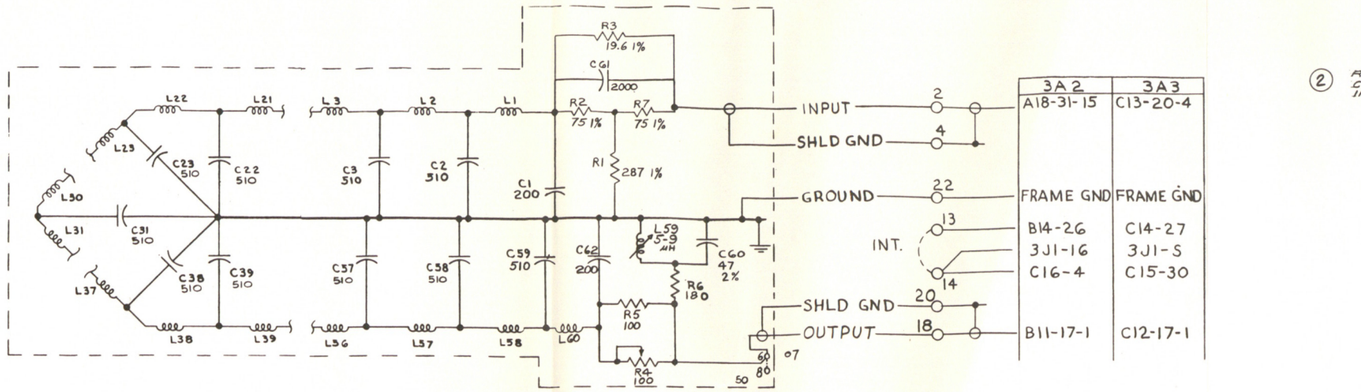




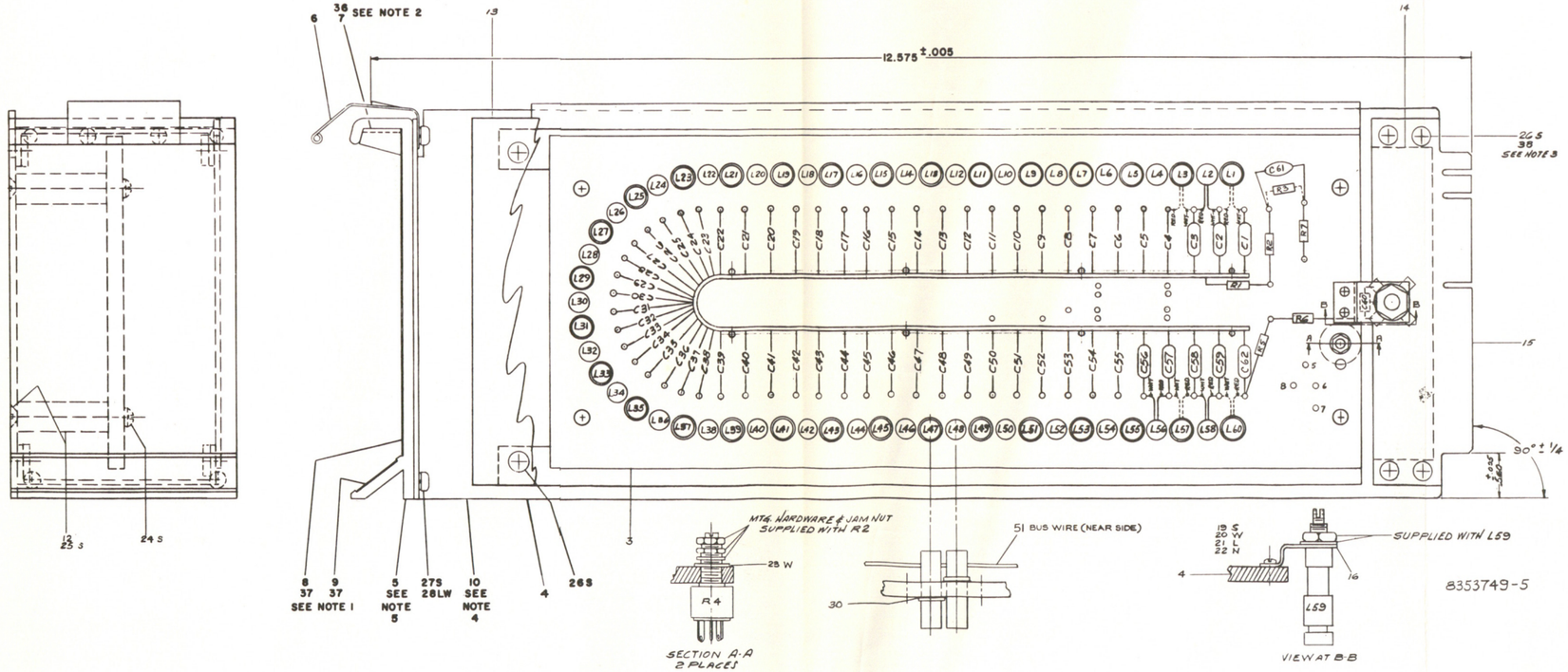
8646700-5

(1) FOR LIST OF PARTS SEE DWG. NO. 8545704

Figure 84—Fixed Delay Line Schematic Diagram for TR-22 Machines



(2) RESISTANCE VALUE IN OHMS, ±5%, 1/2 WATT, EXCEPT AS NOTED. CAPACITANCE VALUE IN MMF, ±1%, 100 VOLTS, EXCEPT AS NOTED. INDUCTANCE VALUES ARE 2.6 μh. EXCEPT AS NOTED.

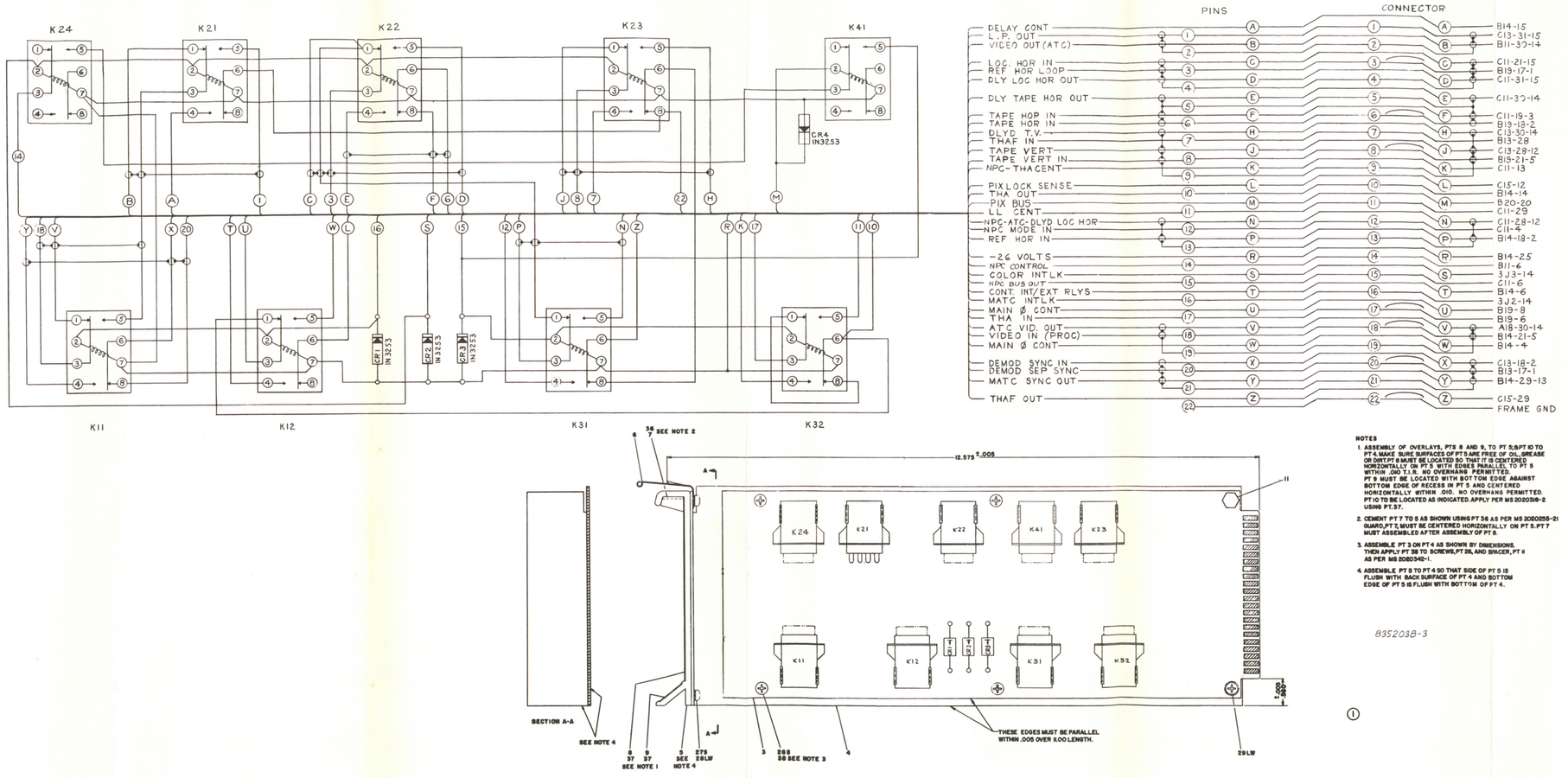


(1) FOR PTS. LIST SEE 8549757-501

NOTES

1. ASSEMBLY OF OVERLAYS, PTS 8 AND 9, TO PT 5. MAKE SURE SURFACES OF PT 5 ARE FREE OF OIL, GREASE OR DIRT. PT 8 MUST BE LOCATED SO THAT IT IS CENTERED HORIZONTALLY ON PT 5 WITH EDGES PARALLEL TO PT 5 WITHIN .010 T.I.R. NO OVERHANG PERMITTED. PT 9 MUST BE LOCATED WITH BOTTOM EDGE AGAINST BOTTOM EDGE OF RECESS IN PT 5 AND CENTERED HORIZONTALLY WITHIN .010. NO OVERHANG PERMITTED. MOISTEN ADHESIVE FILM OF PT 8 AND 9 WITH CLOTH DAMPENED WITH PT 37. THEN PRESS OR ROLL SURFACES TOGETHER TO INSURE GOOD CONTACT AT ALL POINTS.
2. CEMENT PT 7 TO PT 5 AS SHOWN USING PT 36 AS PER MS 2020255. GUARD, PT 7, MUST BE CENTERED HORIZONTALLY ON PT 5. PT 7 MUST BE ASSEMBLED AFTER ASSEMBLY OF PT 8.
3. ASSEMBLE PT 3 ON PT 4 AS SHOWN BY DIMENSIONS. THEN APPLY PT 38 TO SCREWS, PT 26 AND WELD NUT THREADS AS PER MS 2020342-1.
4. ORIENT PT 10 AS SHOWN AND ADHERE TO PT 4 AS SHOWN BY DIMENSIONS. MAKE SURE CONTACTING SURFACE OF PT 4 IS FREE OF OIL, GREASE OR DIRT. REMOVE BACKING FROM PT 10 AND PRESS IN PLACE.
5. ASSEMBLE PT 5 TO PT 4 SO THAT SIDE OF PT 5 IS FLUSH WITH BACK SURFACE OF PT 4 AND BOTTOM EDGE OF PT 5 IS FLUSH WITH BOTTOM OF PT 4.

Figure 85—Fixed Delay Line Module Schematic and Assembly Diagram for TR-3/TR-4 Machines

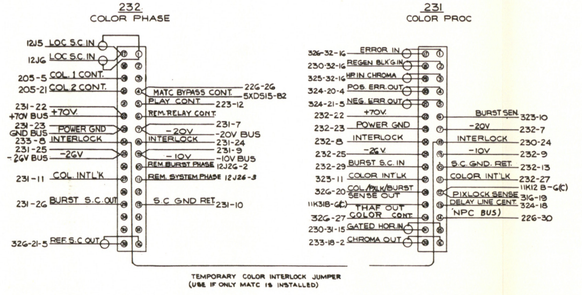


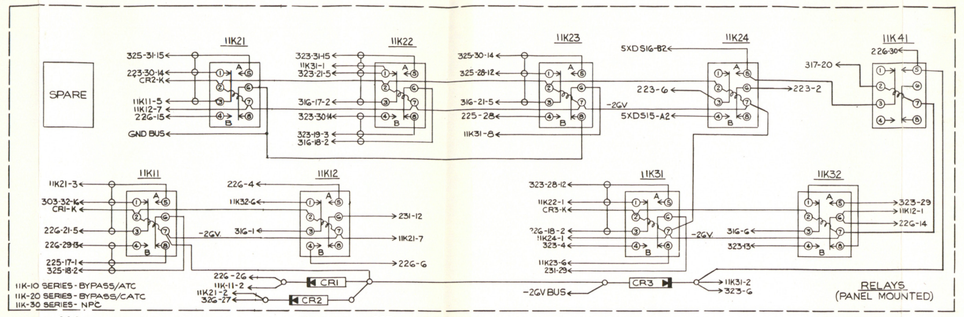
NOTE:
CONNECTOR TERMINALS 'J'-'C', 'G'-'F', '8'-'J', '17'-'U', '18'-'V', '20'-'X' & '22'-'Z' ARE SHORTING TYPE PINS.

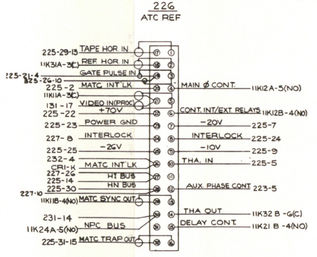
NOTES

1. ASSEMBLY OF OVERLAYS, PT'S 8 AND 9, TO PT 5;8/PT 10 TO PT 4. MAKE SURE SURFACES OF PT'S ARE FREE OF OIL, GREASE OR DIRT.PT 8 MUST BE LOCATED SO THAT IT IS CENTERED HORIZONTALLY ON PT 5 WITH EDGES PARALLEL TO PT 5 WITHIN .010 T.I.R. NO OVERHANG PERMITTED. PT 9 MUST BE LOCATED WITH BOTTOM EDGE AGAINST BOTTOM EDGE OF RECESS IN PT 5 AND CENTERED HORIZONTALLY WITHIN .010. NO OVERHANG PERMITTED. PT 10 TO BE LOCATED AS INDICATED. APPLY PER MS 2020316-2 USING PT.37.
2. CEMENT PT 7 TO 5 AS SHOWN USING PT 36 AS PER MS 2080255-21 GUARD, PT 7, MUST BE CENTERED HORIZONTALLY ON PT 5. PT 7 MUST ASSEMBLED AFTER ASSEMBLY OF PT 8.
3. ASSEMBLE PT 3 ON PT 4 AS SHOWN BY DIMENSIONS. THEN APPLY PT 39 TO SCREWS, PT 38, AND SPACER, PT 6 AS PER MS 2080342-1.
4. ASSEMBLE PT 5 TO PT 4 SO THAT SIDE OF PT 5 IS FLUSH WITH BACK SURFACE OF PT 4 AND BOTTOM EDGE OF PT 5 IS FLUSH WITH BOTTOM OF PT 4.

Figure 86—ATC Relay Module Schematic Diagram for TR-3/TR-4 Machines







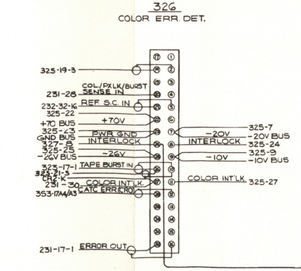
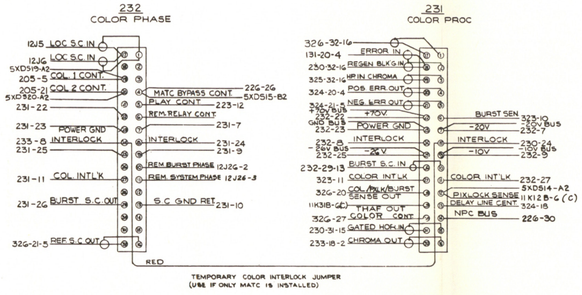
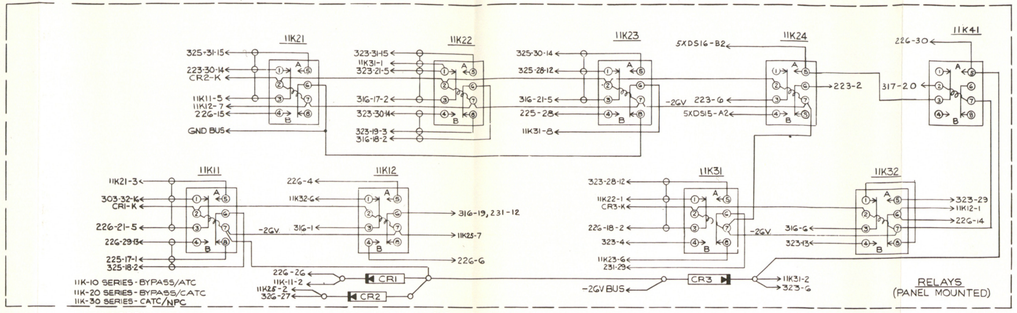
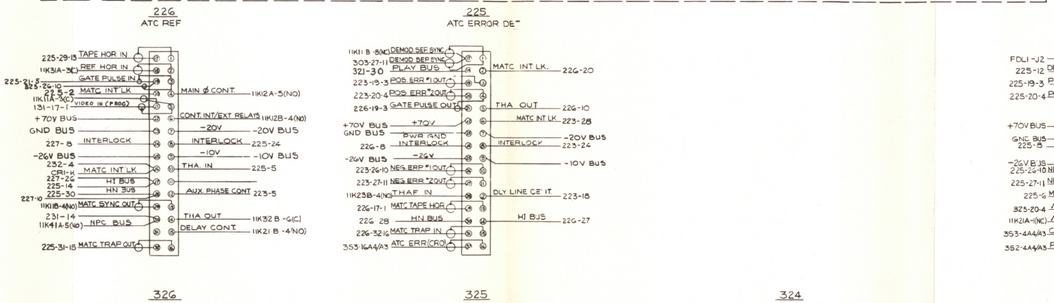


Figure 87—ATC Connection Diagram for TR-22A, B Machines



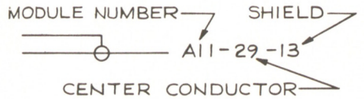




3318133-5

Figure 88—ATC Connection Diagram for TR-22C Machines

TYPICAL COAX CABLE DESTINATIONS



3318070-3

* TR4 ONLY

⌒ SHORTING PIN

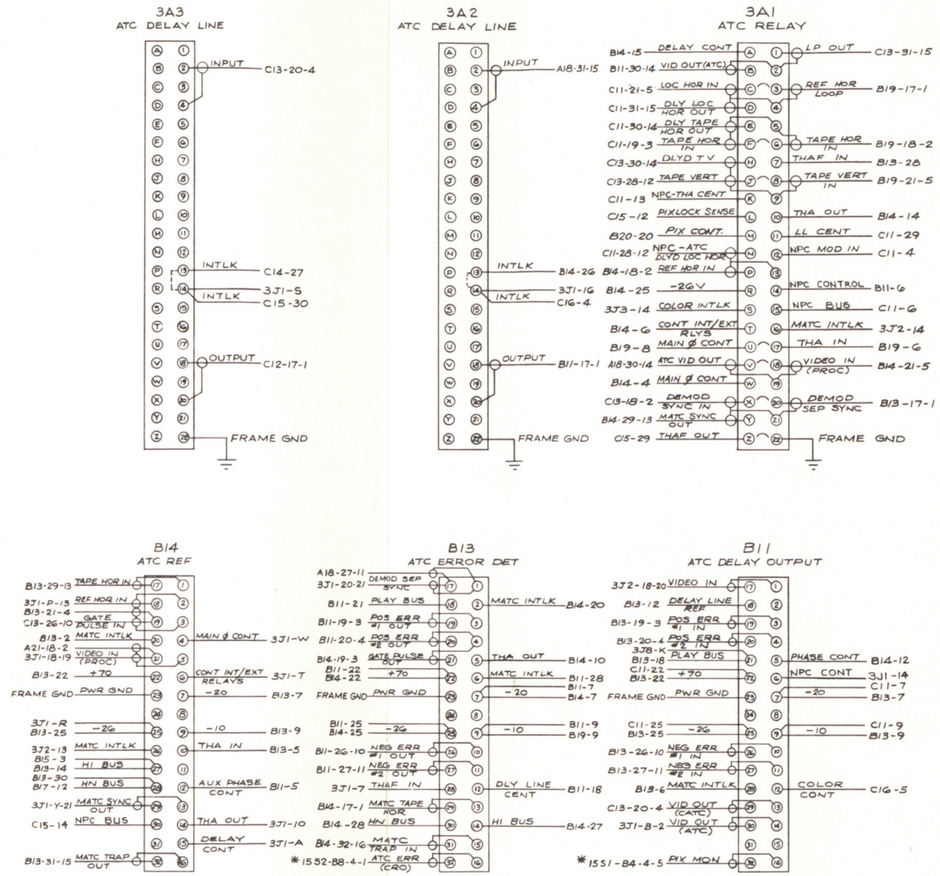
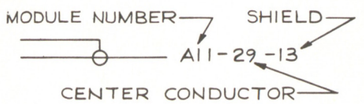


Figure 89—ATC Connection Diagram for TR-3/TR-4 Machines

TYPICAL COAX CABLE DESTINATIONS



331807O-3

* TR4 ONLY
(SHORTING PIN

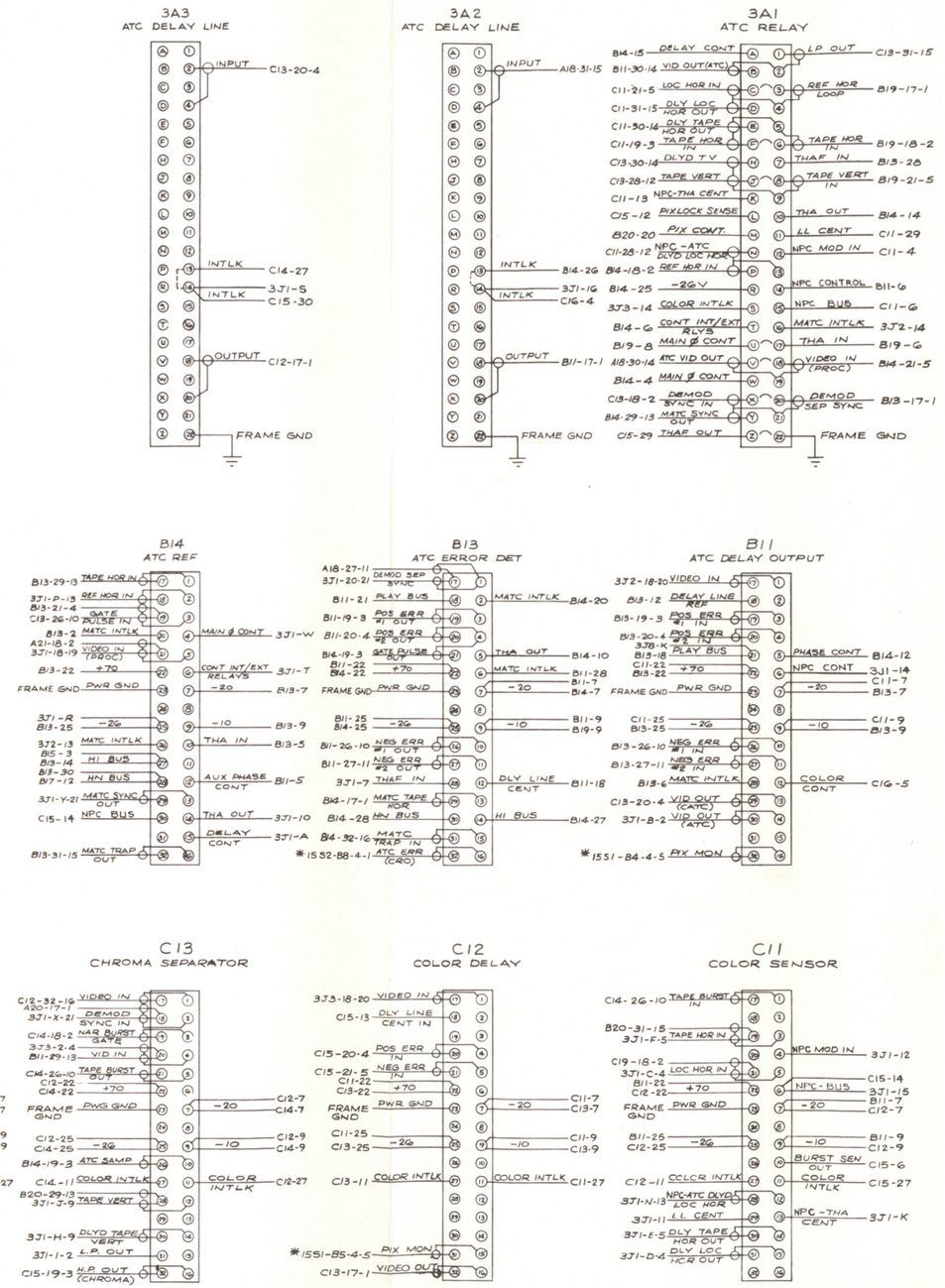
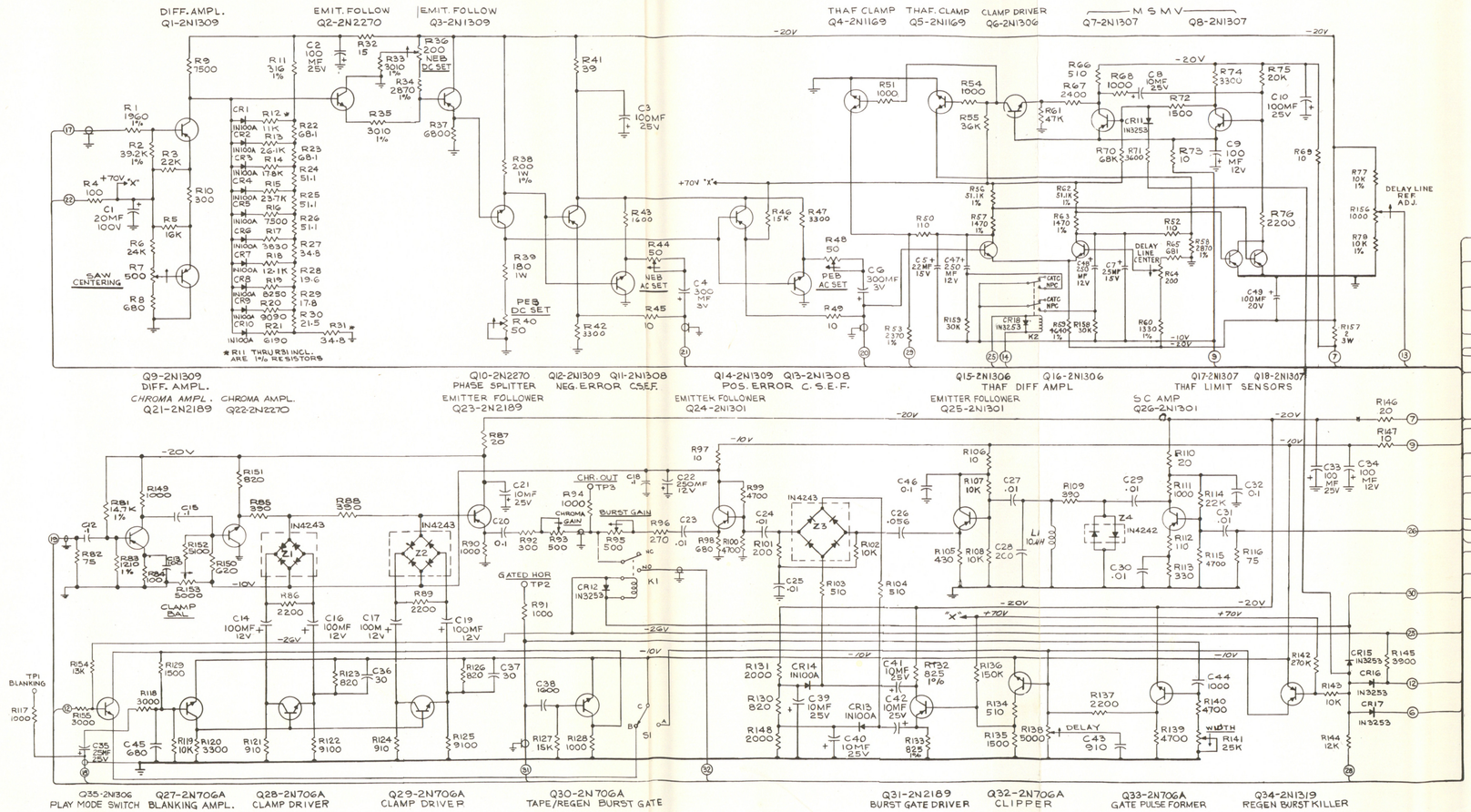
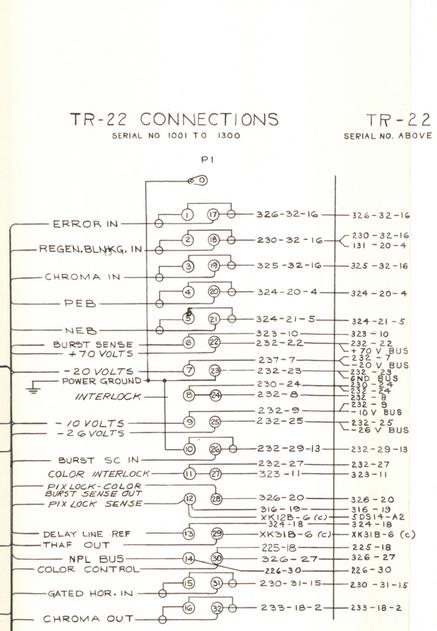


Figure 89—ATC Connection Diagram for TR-3/TR-4 Machines





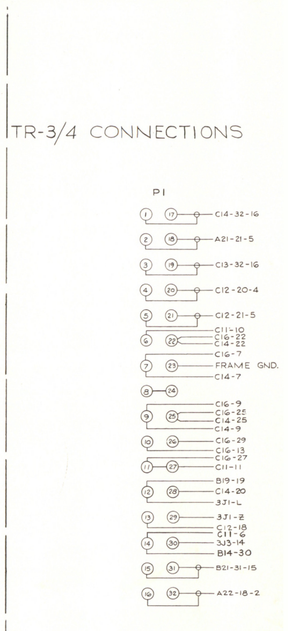


Figure 90—Color Processor Module Schematic Diagram

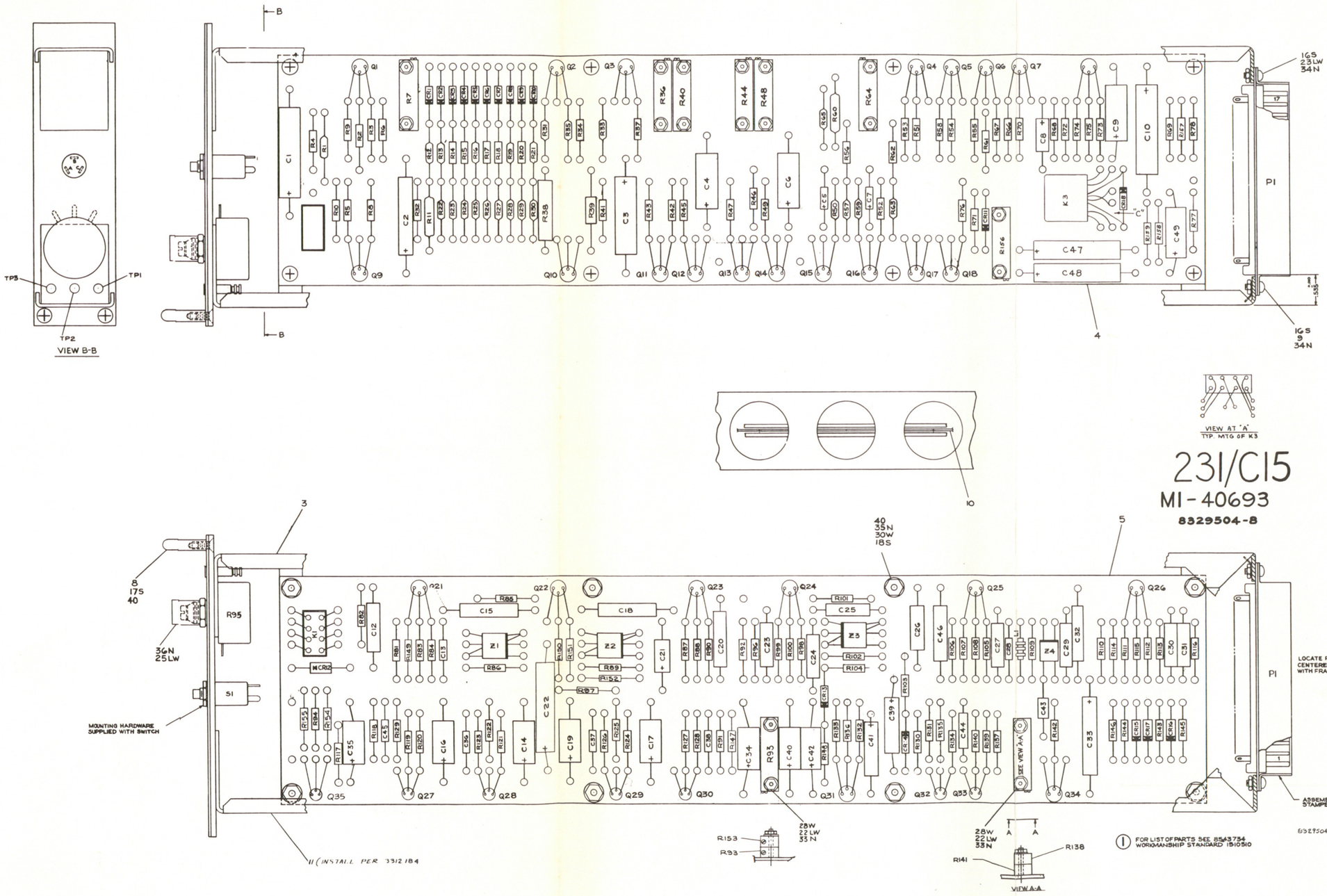


Figure 91—Color Processor Module Assembly Diagram

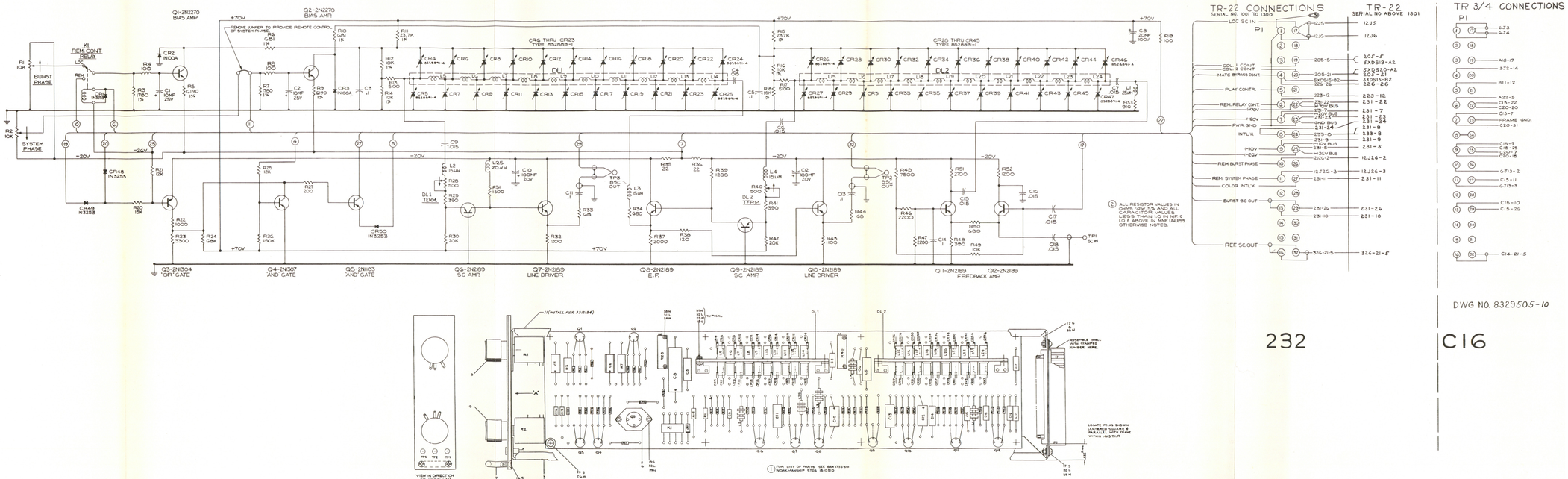
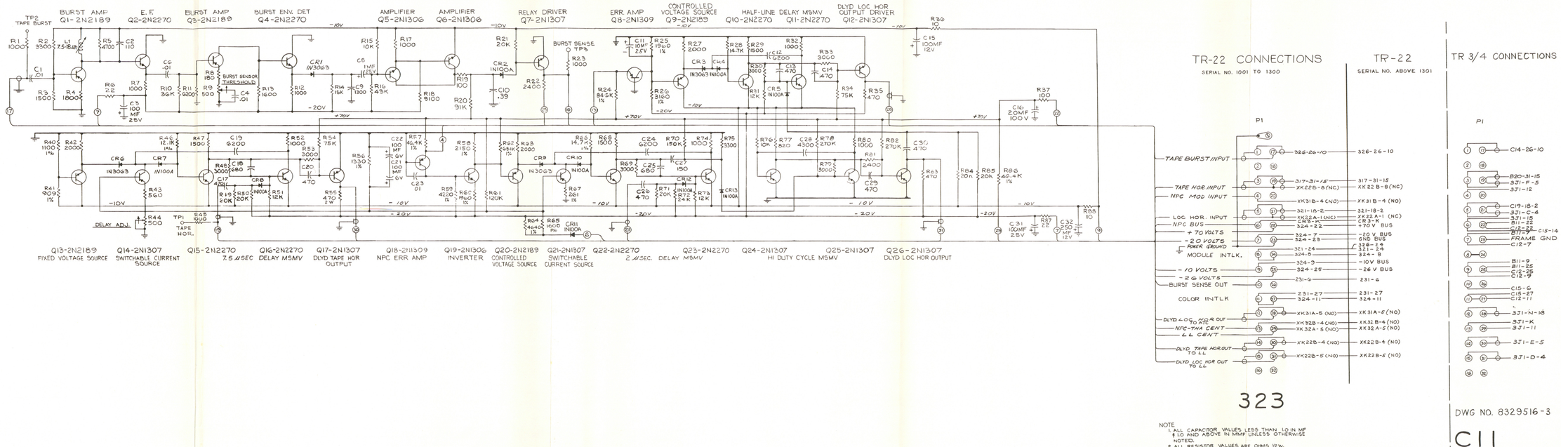


Figure 92—Color Phase Module Schematic and Assembly Diagram



NOTE
1. ALL CAPACITOR VALUES LESS THAN 1.0 IN MF ↑ 1.0 AND ABOVE IN MMF UNLESS OTHERWISE NOTED.
2. ALL RESISTOR VALUES ARE OHMS 1/2 W, ±5% UNLESS OTHERWISE NOTED

Figure 93—Color Sensor Module Schematic Diagram

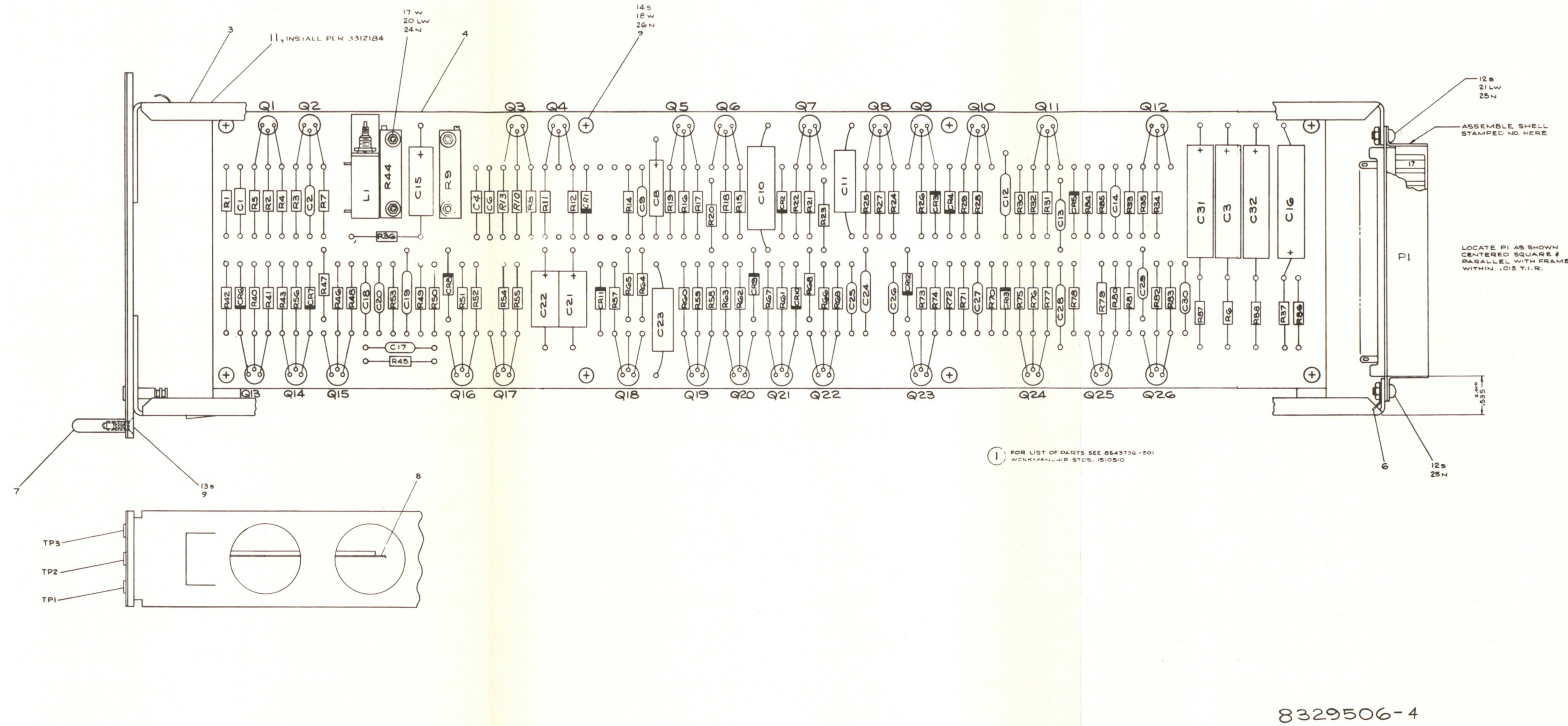
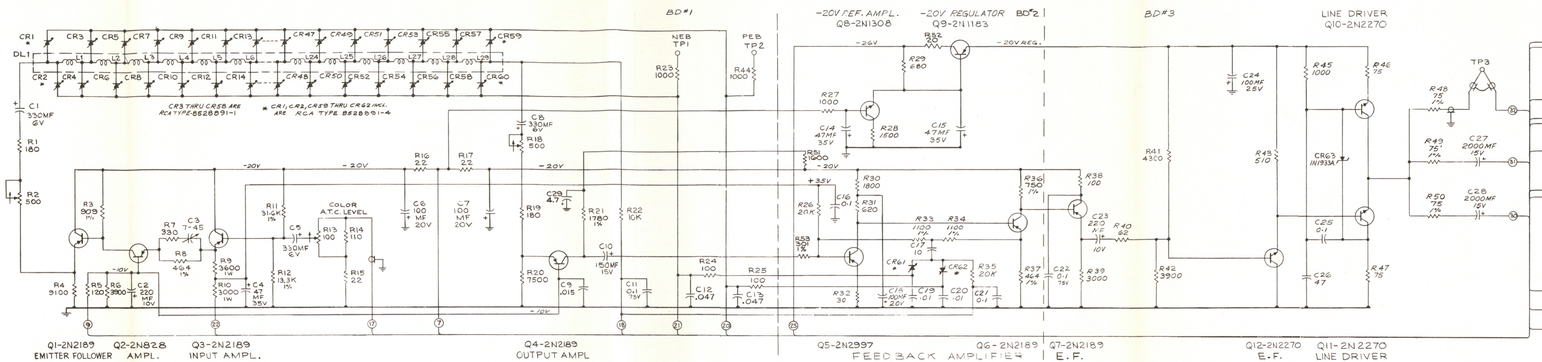


Figure 94—Color Sensor Module Assembly Diagram



TR 3/4 CONNECTIONS

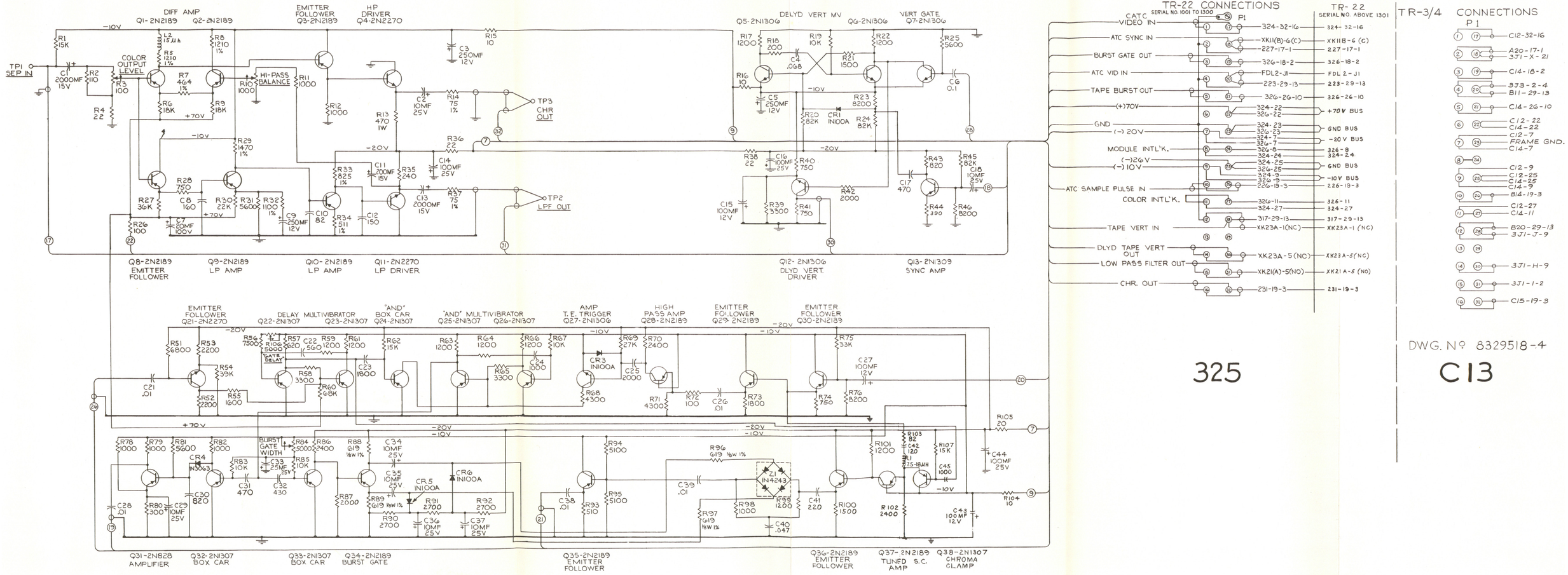
PI

DWG NO. 8329507-7

C12

* TR-4 ONLY

Figure 95—Color Delay Module Schematic and Assembly Diagram

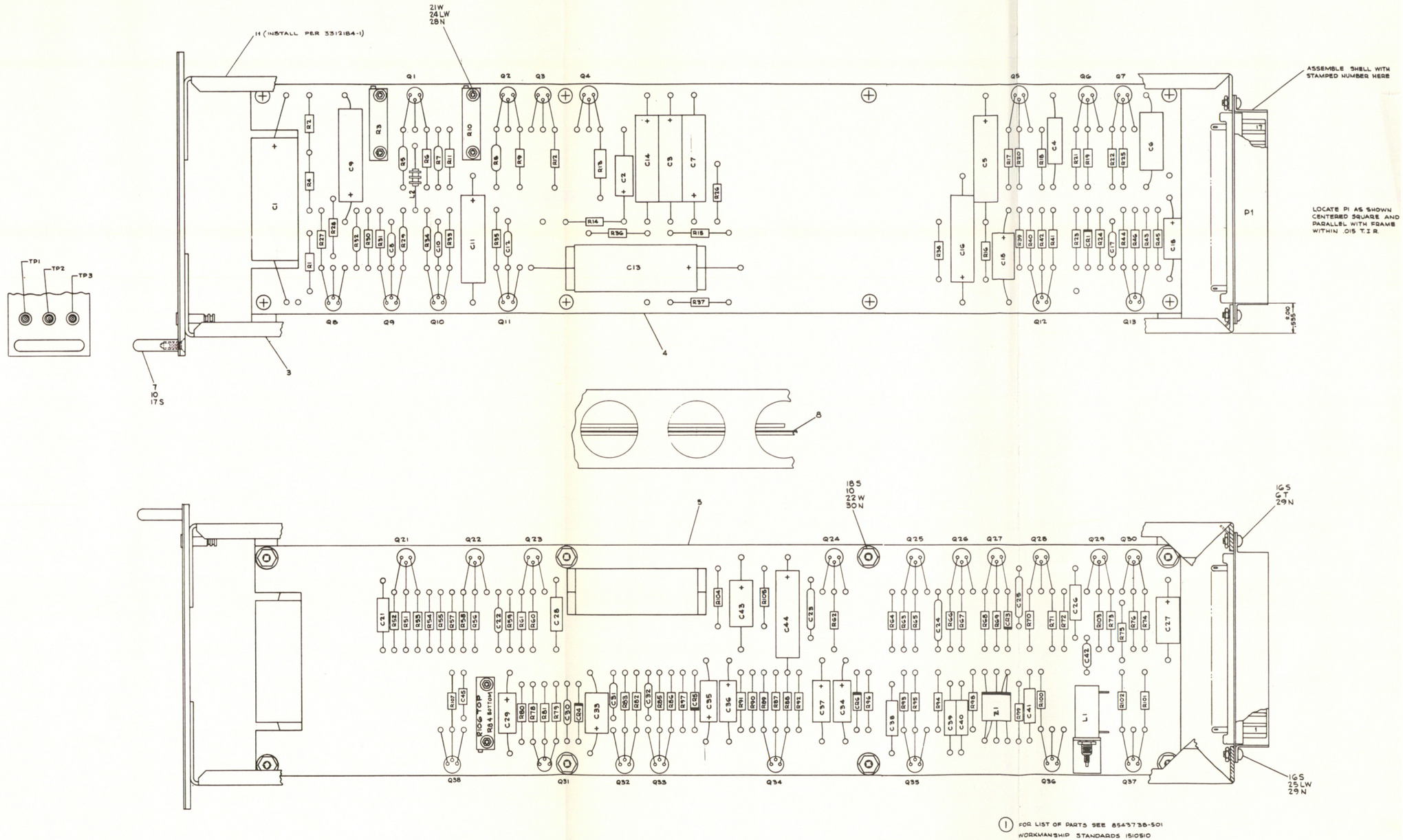


325

DWG. Nº 8329518-4

C13

Figure 96—Chroma Separator Module Schematic Diagram

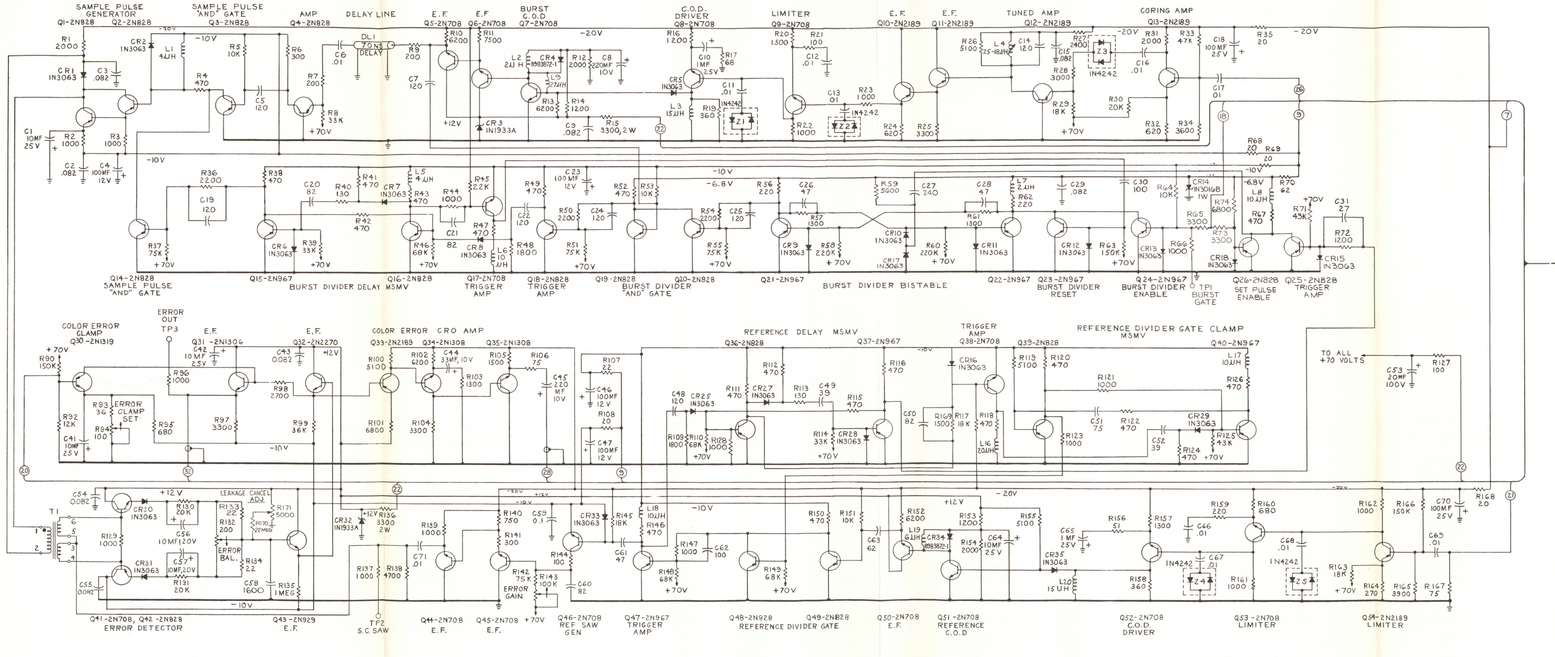


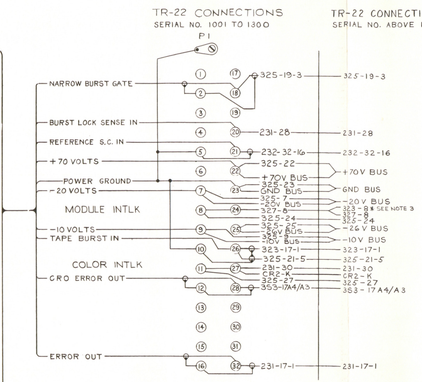
(1) FOR LIST OF PARTS SEE 8543738-501
WORKMANSHIP STANDARDS 1510510

8329508-7

325/C13

Figure 97—Chroma Separator Module Assembly Diagram



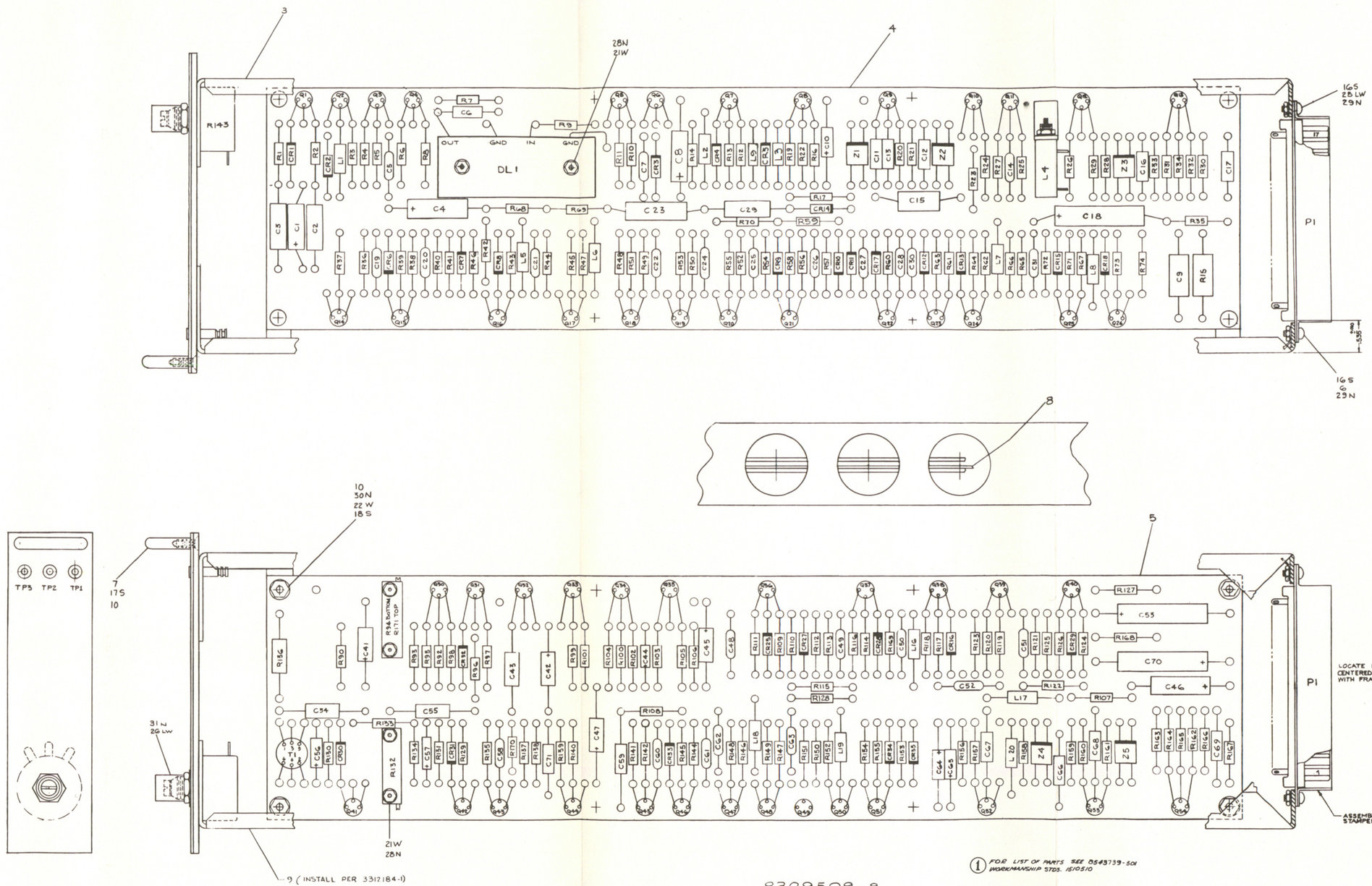


NOTE
1. ALL CAPACITOR VALUES LESS THAN 1.0 IN MF & 1.0 AND ABOVE IN MMF UNLESS OTHERWISE NOTED.
2. ALL RESISTOR VALUES ARE OHMS 1/2 W ± 5% UNLESS OTHERWISE NOTED.
3. JUMPER FROM 326-24 TO 323-5 SHOULD BE REMOVED WHEN COLOR ATC IS ADDED TO TAPE RECORDER

DWG. Nº 8329519-5

C14

Figure 98—Color Error Detector Module Schematic Diagram



8329509-9

326/C14

Figure 99—Color Error Detector Module Assembly Diagram

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